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# PXle-7915 Specifications

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# PXIe-7915 Specifications

## Definitions

**Warranted** specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

**Characteristics** describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Typical** unless otherwise noted.

## Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature of 23 °C ±5 °C
- Installed in chassis with slot cooling capacity ≥58 W

## Digital I/O

Connector	Molex™ Nano-Pitch I/O™
5 V Power	5.0 V DC, ±5%, nominal 50 mA maximum

**Table 1.** Digital I/O Signal Characteristics

Signal	Type	Direction
Multi-gigabit transceivers (MGT) Tx± <3..0>	Xilinx UltraScale GTH	Output
MGT Rx± <3..0>	Xilinx UltraScale GTH	Input
DIO <7..0>	Single-ended	Bidirectional
5 V	DC	Output
GND	Ground	—

## Digital I/O Single-Ended Channels

Number of channels	8
Signal type	Single-ended
Voltage families	3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V
Input impedance	100 k $\Omega$ , nominal
Output impedance	50 $\Omega$ , nominal
Direction control	Per channel
Minimum required direction change latency	200 ns
Maximum output toggle rate	60 MHz with 100 $\mu$ A load, nominal

**Table 2.** Digital I/O Single-Ended DC Signal Characteristics<sup>[1]</sup>

Voltage Family (V)	V <sub>IL</sub> (V)	V <sub>IH</sub> (V)	V <sub>OL</sub> (100 $\mu$ A Load) (V)	V <sub>OH</sub> (100 $\mu$ A Load) (V)	Maximum DC Drive Strength (mA)
3.3	0.8	2.0	0.2	3.0	24
2.5	0.7	1.6	0.2	2.2	18

Voltage Family (V)	V <sub>IL</sub> (V)	V <sub>IH</sub> (V)	V <sub>OL</sub> (100 μA Load) (V)	V <sub>OH</sub> (100 μA Load) (V)	Maximum DC Drive Strength (mA)
1.8	0.62	1.29	0.2	1.5	16
1.5	0.51	1.07	0.2	1.2	12
1.2	0.42	0.87	0.2	0.9	6

## Digital I/O High-Speed Serial MGT<sup>[2]</sup>

Data rate	500 Mbps to 16.375 Gbps, nominal
Number of Tx channels	4
Number of Rx channels	4

Figure 1. Digital I/O Connector

Reserved	A1	B1	5 V
GND	A2	B2	GND
MGT Rx+ 0	A3	B3	MGT Tx+ 0
MGT Rx- 0	A4	B4	MGT Tx- 0
GND	A5	B5	GND
MGT Rx+ 1	A6	B6	MGT Tx+ 1
MGT Rx- 1	A7	B7	MGT Tx- 1
GND	A8	B8	GND
DIO 4	A9	B9	DIO 6
DIO 5	A10	B10	DIO 7
GND	A11	B11	GND
MGT REF+ / DIO 0	A12	B12	DIO 2
MGT REF- / DIO 1	A13	B13	DIO 3
GND	A14	B14	GND
MGT Rx+ 2	A15	B15	MGT Tx+ 2
MGT Rx- 2	A16	B16	MGT Tx- 2
GND	A17	B17	GND
MGT Rx+ 3	A18	B18	MGT Tx+ 3
MGT Rx- 3	A19	B19	MGT Tx- 3
GND	A20	B20	GND
5.0 V	A21	B21	Reserved

## MGT TX± Channels<sup>[3]</sup>

Minimum differential output voltage <sup>[4]</sup>	170 mV pk-pk into 100 Ω, nominal
I/O coupling	AC-coupled, includes 100 nF capacitor

## MGT RX± Channels

<b>Differential input voltage range</b>	
≤ 6.6 Gb/s	150 mV pk-pk to 2000 mV pk-pk, nominal
> 6.6 Gb/s	150 mV pk-pk to 1250 mV pk-pk, nominal
Differential input resistance	100 Ω, nominal
I/O coupling	DC-coupled, requires external capacitor

## Reconfigurable FPGA

FPGA	Xilinx KU060
LUTs	331,680
DSP48 Slices (25 × 18 multiplier)	2,760
Total block RAM	38.0 Mb
Default timebase	80 MHz
Timebase reference sources	PXI Express 100 MHz (PXIe_CLK100)

Data transfers	MGT
Number of DMA channels	60
Connection resources	PXI triggers, PXI_CLK10, PXI star trigger, PXIe_DStarB, PXIe_DStarC, and PXIe_Sync100



**Note** The preceding specifications describe the total number of FPGA resources available on the part. The number of resources available to the user is slightly lower, as some FPGA resources are consumed by board-interfacing IP for PCI Express, device configuration, and various board I/O. For more information, contact NI support.



**Note** For FPGA designs using the majority of KU040 or KU060 FPGA resources while running at clock rates over 150 MHz, the module may require more power than is available. If the module attempts to draw more than allowed per its specification, the module protects itself and reverts to a default FPGA personality. Refer to the getting started guide for your module or contact NI support for more information.

## Onboard DRAM

Memory size	4 GB (2 banks of 2 GB)
DRAM clock rate	1064 MHz
Physical bus width	32 bit
LabVIEW FPGA DRAM clock rate	267 MHz
LabVIEW FPGA DRAM bus width	256 bit per bank

Maximum theoretical data rate	17 GB/s (8.5 GB/s per bank)
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## Driver and Application Software

This device is supported in NI LabVIEW Instrument Design Libraries for FlexRIO (instrument design libraries). Instrument design libraries allow you to configure and control the device.

The instrument design libraries provide programming interfaces, documentation, and sample projects for LabVIEW and LabVIEW FPGA Module.

## Bus Interface

Form factor	PCI Express Gen-3 x8
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## Maximum Power Requirements



**Note** Power requirements depend on the contents of the LabVIEW FPGA VI used in your application.

+3.3 V	3 A
+12 V	4 A
Maximum total power	58 W

## Physical

Dimensions (not including connectors)	18.8 cm × 12.9 cm (7.4 in. × 5.1 in.)
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Weight	190 g (6.7 oz)
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## Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

## Operating Environment

Ambient temperature range	0 °C to 55 °C <sup>[5]</sup>
Relative humidity range	10% to 90%, noncondensing

## Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 4 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

## Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse
<b>Random vibration</b>	

Operating	5 Hz to 500 Hz, 0.3 g <sub>rms</sub>
Nonoperating	5 Hz to 500 Hz, 2.4 g <sub>rms</sub>

<sup>1</sup> Voltage levels are guaranteed by design through the digital buffer specifications.

<sup>2</sup> For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

<sup>3</sup> For detailed FPGA and High-Speed Serial Link specifications, refer to Xilinx documentation.

<sup>4</sup> 800 mV pk-pk when transmitter output swing is set to the maximum setting.

<sup>5</sup> The PXIe-7915 requires a chassis with slot cooling capacity  $\geq 58$  W. Not all chassis with slot cooling capacity  $\geq 58$  W can achieve this ambient temperature range. Refer to the [PXI Chassis Manual](#) for specifications to determine the ambient temperature ranges your chassis can achieve.