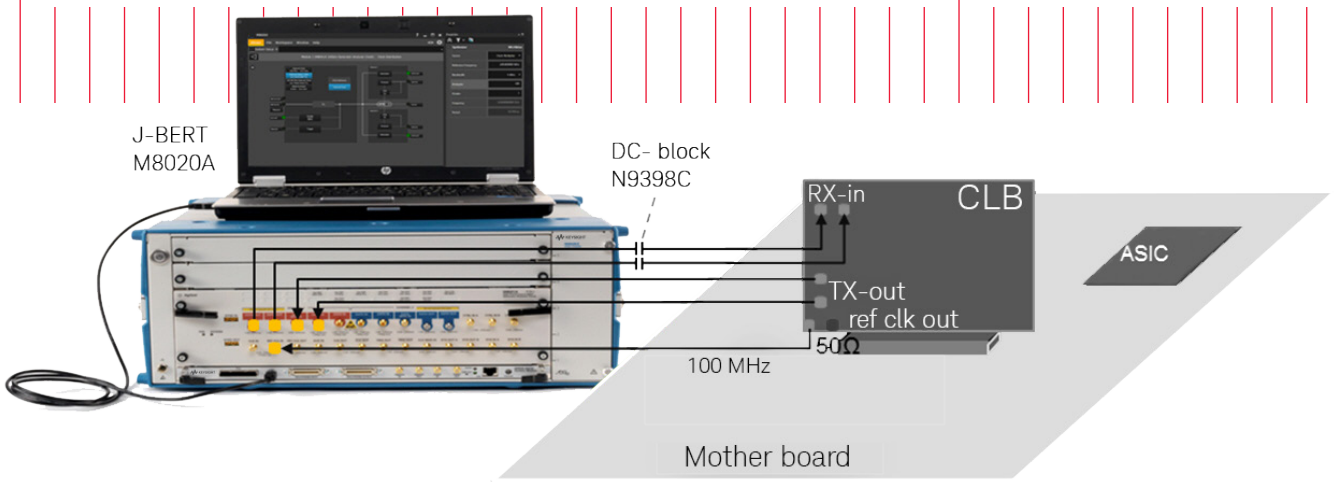
Keysight Technologies
Master Your Next PCI® Express Test
J-BERT M8020A High-Performance BERT

Application Brief



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Disclaimer

It is not within the scope of this document to explain the reasons for receiver testing or to provide detailed information on the calibration of receiver stress signals for PCI Express. Very detailed application notes covering those topics for PCI Express for 5 GT/s as well as 8 GT/s are available for download on **www.keysight.com**.

- Receiver testing for PCI Express 5 GT/s Base specification as well as CEM specification:
  - Publication number: 5990-3233EN
  - **http://literature.cdn.keysight.com/litweb/pdf/5990-3233EN.pdf**
- Receiver testing for PCI Express 8 GT/s Base Specification:
  - Publication number: 5990-6599EN
  - **http://literature.cdn.keysight.com/litweb/pdf/5990-6599EN.pdf**
- Receiver testing for PCI Express 8 GT/s CEM Specification:
  - Publication number: 5990-9208EN
  - **http://literature.cdn.keysight.com/litweb/pdf/5990-9208EN.pd**f

Method of Implementations for PCI Express for Keysight Technologies, Inc. test equipment are available on www.pcisig.com within the member section.

This document refers to PCI Express Base Specification Revision 4.0 which was not finalized at release of this document. Therefore specifications and methodologies for 16 GT/s can differ from the ones mentioned in this document.

Introduction

The receiver (RX) specification for PCI Express evolved with specification revisions and data rate increases. For instance the reference point for receiver parameters is for 2.5 GT/s and 5 GT/s outside the chipset hosting the PCI Express RX while for 8.0 GT/s and 16 GT/s the reference point is within the chipset. The requirements for a stress signal used to test a receiver are developed to a higher detail and complexity level. Three major PCI Express specification layers and different device under test (DUT) categories as well as different operation modes result in setup and test differences. Finding a receiver test platform which can master this variety is difficult. The goal of this document is to provide an overview of PCI Express receiver testing for the different transfer speeds as well as different specifications and to present the test setup based on the J-BERT M8020A.

PCI Express Specifications

The PCI Express Base Specification is the foundation for the PCI Express specification frame work. From a physical layer perspective it specifies transmitter, channel, and receiver parameters as well as possible clocking architectures and the logical sub block. Every PCI Express use model refers to the base specification. The base specification is most relevant for chipset testing. Synchronous operation as well as asynchronous operation is supported by the base specification. Three different types of clocking architectures are possible: common reference clock (CC) which is synchronous, data clocked (DC) which can be synchronous or asynchronous, or independent reference clock (IR) which is asynchronous. Originally, asynchronous operation was allowed in the absence of spread spectrum clocking (SSC) only. Asynchronous operation in the presence of SSC was introduced early in 2013. Separate reference clock no SSC (SRNS) is used to describe asynchronous operation without SSC and separate reference clock independent SSC (SRIS) is used to describe asynchronous operation with SSC. Different test requirements are defined for 8 GT/s and 16 GT/s RX testing for synchronous and asynchronous operation.

The largest PCI Express use model is most likely the PCI Express extension slot which is defined by the PCI Express Card Electromechanical (CEM) specification. Two different device types need to be considered for receiver testing: add-In cards (AIC) and mainboards (system). CEM uses synchronous operation only and it is the only PCI Express ecosystem providing a mandatory compliance certification program including physical layer tests. Every device found on the PCI-SIG® integrators list had to pass compliance testing at one of the PCI-SIG compliance workshops. The required physical layer compliance tests are defined in the PCI Express Architecture PHY Test Specification (CTS). The CTS tests are designed to be manageable in a workshop environment. As a result, receiver testing according to the CTS can be less stringent and less complete than receiver testing according to the base specification.

Other interest groups start using PCI Express technology. The Serial ATA International Organization introduced SATA Express which uses the physical layer of PCI Express. SATA Express uses synchronous operation as well as asynchronous operation. If SATA Express devices are connected to the host via a cable, asynchronous operation
is required.

M-PCIe, however, replaces the physical layer of PCI Express by the PHY layer defined for M-PHY®. Receiver testing therefore has to be performed according to the M-PHY specification and not the PCI Express specification. M-PHY is a physical layer defined by the MIPI Alliance.

PCI Express Receiver Test Requirements

Test requirements and calibration methodologies are not the same for the different transfer rates. The specification reference point moved into the chip starting with revision 3.0 and composition of the stress signal became more complex. The methodology describing the inter symbol interference (ISI) channel to be used for receiver testing differs for 2.5 GT/s, 5 GT/s, and 8 GT/s/16 GT/s.

PCI Express provides backward compatibility. Therefore a device capable of a higher data rate needs to be compliant to the lower data rates, too.

PCI Express 2.5 GT/s

Base specification	CEM specification	PHY test specification
Yes	Yes	No

Receiver specifications are defined at receiver pins. Specifications are identical for different clock architectures and synchronous or asynchronous operation modes. A simple receiver mask is defined only. In the absence of a random jitter (RJ) specification, solutions today usually use the RJ defined for 5 GT/s. Base specification testing does not require de-emphasis but testing according to CEM does.

Stressor mix:

- ISI via an external channel. ISI should be the major DJ component. CEM testing requires the PCI-SIG Compliance Base Board (CBB) and Compliance Load Board (CLB). CBB for gen1 and gen2 needs to be modified for receiver testing. Modification details are outlined in the PCI Express receiver test application note, pub number 5990-3233EN, **http://literature.cdn.keysight.com/litweb/pdf/5990-3233EN.pdf**
- RJ
- Sinusoidal jitter (SJ) to supplement ISI for necessary eye closure
- Common mode sinusoidal interference (CM-SI), base specification only

PCI Express 5.0 GT/s

Base specification	CEM specification	PHY test specification
Yes	Yes	No

Receiver specifications are defined at receiver pins. The base specification defines different parameters for CC and DC based receiver designs. The CEM specification does not apply CM-SI but adds a secondary high frequency jitter tone. Residual SSC (rSSC) is introduced for CC use cases; rSSC is a triangular phase modulation which is applied to the stressed data signal only but not to the reference clock. It represents the worst case delta a receiver can experience between SSC on the reference clock and SSC on the incoming data signal.

Stressor mix:

- ISI via an external channel. ISI should be the major DJ component. CEM testing requires the PCI-SIG Compliance Base Board (CBB) and Compliance Load Board (CLB). CBB for gen1 and gen2 needs to be modified for receiver testing. Modification details are outlined in the PCI Express receiver test application note, pub number 5990-3233EN, **http://literature.cdn.keysight.com/litweb/pdf/5990-3233EN.pdf**
- Spectral filtered RJ (sRJ) with higher RJ amplitude for frequency spectrum up to 1.5 MHz and lower RJ amplitude for frequency spectrum between 1.5 MHz and 100 MHz
- SJ to supplement ISI for necessary eye closure
- SSC:
  - rSSC is used for CC based implementation except for CEM based system tests since SSC is defined by the system's reference clock
  - SSC is used for DC based implementations
- CM-SI, base specification only
- Secondary high frequency SJ tone for CEM specification only

PCI Express 8.0 GT/s

Base specification	CEM specification	PHY test specification
Yes	Yes	Yes

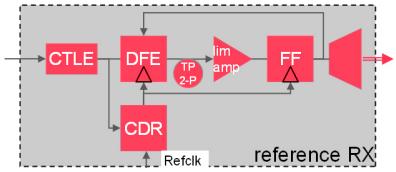


Figure 3.3-1. 8 GT/s RX specification reference point is within a reference receiver

While receiver designs operating at 2.5 GT/s and 5.0 GT/s could be implemented without receiver equalization (EQ) and rely solely on TX equalization, the increased transmission rate via basically the same channel makes RX equalization necessary and consequently testing of receiver gain more important. Transmitter equalization was extended with pre-shoot next to de-emphasis. The Link Training Status State Machine (LTSSM) was extended by a mechanism which allows a RX to request TX EQ changes during link training.

The receiver specifications are more thorough and are defined within the receiver after CTLE and DFE. This reference point is referred to as TP2-P. As a consequence of this definition point shift, embedding of a behavioral RX package as well as simulation of the equalizer stages and clock recovery are required for the stress signal calibration.

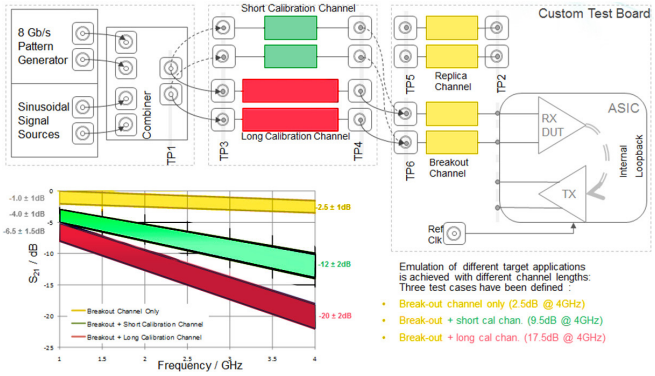


Figure 3.3-2. Base specification test points for 8 GT/s receiver calibration

Base specification and CEM specification / PHY Test Specification have chosen different simulation and calibration approaches. The concepts of sRJ and rSSC were abandoned for 8 GT/s.

A calibration according to the base specification simulates the entire receiver stress signal based on a channel measurement via a step response and stressors are input parameters to the simulation. The simulation tool recommended is SEASIM, a python script available from the PCI-SIG webpage. Based on the simulation, the stressor parameters required to achieve the necessary eye height (EH) and eye width (EW) have to be determined. The stressors are then calibrated to the parameters determined by the simulation at more suitable test points to reduce measurement uncertainty as much as possible.

The base specification receiver test is broken down into two major tests: stressed voltage test and stressed jitter test. The stressed voltage test is performed for three different test cases, no channel, short channel, and long channel (according to Figure 3.3-2) while the stressed jitter test uses the long channel only. The stressed voltage test puts more emphasis on EH and requires an amplitude stressor in the form of a differential mode sinusoidal interference (DM-SI) and CM-SI in addition to jitter stressors. As a result a complete base specification receiver test for 8 GT/s is comprised of four different receiver tests.

With the addition of SRIS to the base specification two jitter tolerance masks were introduced.

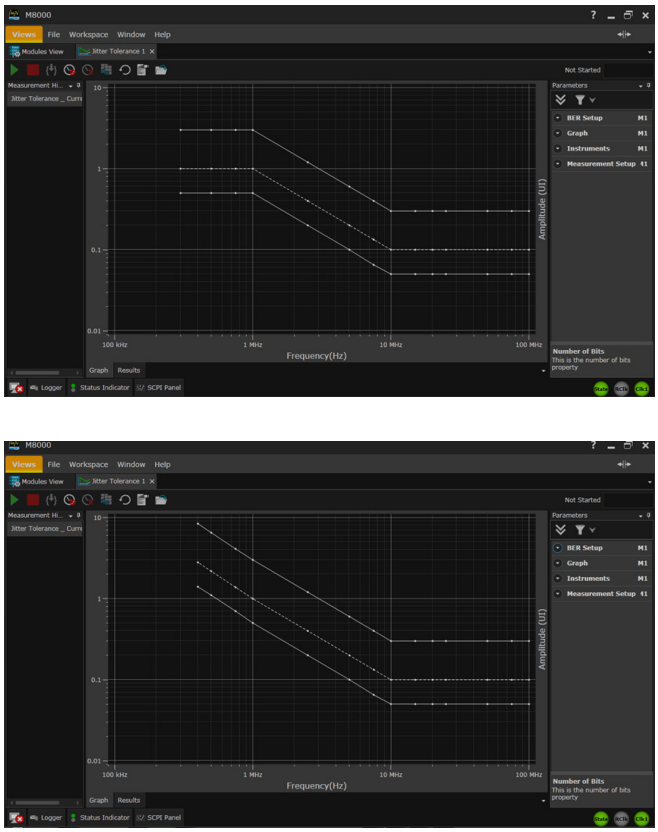


Figure 3.3-4. 8 GT/s Jitter tolerance templates for CC (upper graph) and DC/IR (lower graph) with min and max search envelope

CC is tested without SSC except if a system is tested and SSC cannot be turned off. SRNS is always tested without SSC and SRIS is tested with SSC activated but the modulation profile differs for the stressed voltage test and stressed jitter test. In the case of a stressed voltage test a triangular down spread is used while a sinusoidal down spread is used for stressed jitter test.

The CEM / PHY Test Specification calibration procedure is based on a measurement of the stress signal with activated stressors. The test channel for the calibration is defined by the CCB + CLB combination required for AIC or system testing. The comparable test point in base specification terms would be TP2. A measurement analysis software called SIGTEST is used to determine RJ, SJ, EH, and EW. SIGTEST embeds the behavioral RX package and simulates equalization stages and clock recovery according to

the reference receiver. This approach seems to be more natural compared to the base specification approach but has to deal with higher measurement uncertainties and thus measurements have to be repeated a few times, sorted for outliers, and averaged to achieve usable data. SIGTEST is available via the PCI-SIG webpage as well as the CBB and CLB required for an 8 GT/s receiver test. The 8 GT/s CBB allows receiver testing without modification of the CBB and comprises a riser to simulate the worst case channel.

The CEM / PHY Test Specification receiver tests combines the long channel stressed voltage test and stress jitter test into one receiver test to reduce test time at workshops. For the same reason it does not check the SJ template outlined in the base specification. An additional difference is that CM-SI is not part of the stressor mix to reduce the complexity of the test setup required at workshops. To fit test time into a typical workshop time slot the pass fail criterion chosen does not test for a ber ≤ 10^{-12} with a confidence level of 95% but uses a fixed test time equivalent to 10^{12} compared bits and pass or fail is determined by the number of errors measured. Up to one error constitutes a pass and more than one error a fail. An additional short channel test for AICs is informative. For this test the gen3 CBB + riser are replaced by a gen2 CBB but the same stressor settings used for the long channel test are used.

An additional test category was introduced to test the active TX equalization (EQ) negotiation. The so called “transmitter link equalization test” checks the transmitter’s ability to act upon receiver requests and the “receiver link equalization test” tests if the negotiation yielded in a successful link. To verify this, a jitter tolerance test is performed using the TX EQ settings from the results of the negotiation. The receiver link equalization test is different from a standard jitter tolerance in terms of the method used to train the DUT into loopback. Loopback for a standard jitter tolerance can be forced or trained through the LTSSM state configuration while for the receiver link equalization test the receiver needs to be trained through “L0” and “recovery” states.

Stressor mix:

- ISI via an external channel. CEM testing requires PCI-SIG Compliance Base Board (CBB), riser and Compliance Load Board (CLB) for gen3 for long channel and CBB gen2 for short channel test.
  - RJ with 10 MHz high-pass filter applied
  - SJ, different jitter tolerance masks for CC and SRNS/SRIS
- SSC, SRIS only:
  - Triangular down spread @ 33 kHz for stressed voltage test
  - Sinusoidal down spread @ 33 kHz for stressed jitter test
- DM-SI
- CM-SI, base specification only

PCI Express 16 GT/s

Base specification	CEM specification	PHY test specification
Yes	Yes	Likely, work on PHY Test Specification has not been started at release of this document

PCI Express revision 4.0 will include 16 GT/s. The specification is not released and not stable at the release of this document. But PCI-SIG workgroups have started work on revision 4.0 and the 16 GT/s receiver specification will likely follow the methods of the 8 GT/s receiver calibration.

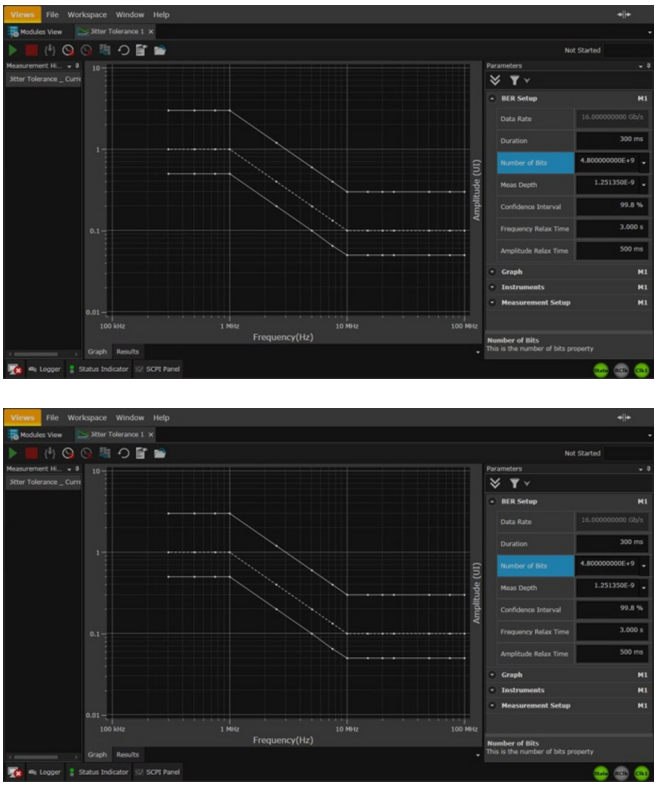


Figure 3.4-1. 16GT/s Jitter tolerance templates for CC (upper graph) and DC/IR (lower graph)

Preliminary stressor mix:

- ISI via an external channel. CEM testing will most likely require test fixtures developed and provided by PCI-SIG.
- RJ with 10 MHz high-pass filter applied
- SJ, different jitter tolerance masks for CC and SRNS/SRIS
- SSC, SRIS only:
  - Triangular down spread @ 33 kHz for stressed voltage test
  - Sinusoidal down spread @ 33 kHz for stressed jitter test
- DM-SI
- CM-SI, base specification only

Stress Signal Overview Table and J-BERT M8020A Stress Sources

x..required
(x)..not required for compliance but recommended for characterization

Jitter type	M8020A stress source	2.5 GT/s CC	2.5 GT/s DC IR[1]	5.0 GT/s CC	5.0 GT/s DC IR[1]	8.0 GT/s CC	8.0 GT/s DC IR[1]	16 GT/s7 CC	16 GT/s7 DC IR[1]	Comment
RJ	RJ	x	x	–	–	x 10 MHz high pass filter		x 10 MHz high pass filter		
Two band spectrally filtered RJ	sRJ	–	–	x lower RJ up to 1.5 MHz and higher RJ band from 1.5 MHz to 100 MHz		–		–		
SJ	HF-PJ1 and LF PJ	–	(x)	–	(x)	x	x	x	x	
Secondary SJ tone	HF-PJ2	–	–	x[2]	x[2]	–	–	–	–	
SSC	SSC	(x)[3]	(x)[3]	(x)[3]	(x)[3]	(x)[3]	x[4, 5]	(x)[3]	x[4, 5]	SSC only for CC or SRIS[8] but not SRNS[9]
ISI	External channel	≈100 mUI		≈440 mUI 5:1 amplitude ratio definition		3 test cases: –3 dB @ 4 GHz –12 dB @ 4 GHz –20 dB @ 4 GHz		3 test cases: –3 dB @ 8 GHz –12 dB @ 8 GHz –20 dB @ 8 GHz		Examples for external channels: N5990A-014 PCI Express 8 GT/s ISI traces M8048A universal ISI traces Artek CLE1000-A2 adjustable ISI instrument
DM-SI	DM-SI	–	–	–	–	x	x	x	x	
CM-SI	CM-SI	x[1]	x[1]	x[1]	x[1]	x[1]	x[1]	x[1]	x[1]	

1. Base specification only
2. CEM specification only
3. ASIC and AIC
4. Stressed jitter test: down spread sinusoidal modulation @ 33 kHz
5. Stressed voltage test: down spread triangular modulation @ 33 kHz
6. Probably down spread sinusoidal modulation @ 33 kHz
7. Specification was not finalized at release of this document
8. SRIS – Separate Reference Clock Separate SSC, link partners operate in separate clock domains and SSC is applied. RX clocking architecture can be DC or IR. SRIS was introduced after specification revision 3.0 via ECN and is part of specification revision 3.1.
9. SRNS – Separate Reference Clock No SSC, link partners operate in separate clock domains but SSC is not allowed. RX clocking architecture can be DC or IR. In earlier specification revisions SRNS was referred to as DC in asynchronous operation mode which did not allow the usage of SSC.

Summary receiver specification

The J-BERT M8020A has all non ISI stressors built in which are required for all transfer rates, clocking operation modes, device types, PCI Express base, and CEM and PHY Test Specification. ISI is achieved by adding channels to the test setup. In the case of CEM / PHY Test Specification the channels are defined by the PCI-SIG and realized through respective test fixtures (CBBs and CLBs). For the base specification Keysight's N5990A-014 and M8048A fixed ISI channels or Artek's CLE1000-A2 adjustable ISI channel can be used.

PCI Express Receiver Test Setups Based on J-BERT M8020A

The applicable specification defined by the target device, transfer speeds, and clocking operations mode determine the test setup required.

Base specification

With its requirement for simultaneous common mode and differential mode sinusoidal interference the 8 GT/s and 16 GT/s test setups are the most complicated ones in terms of stressors. Most receiver test solutions so far, including the J-BERT N4903B based setup, required additional instruments to complete the stressor set offered by the BERT.

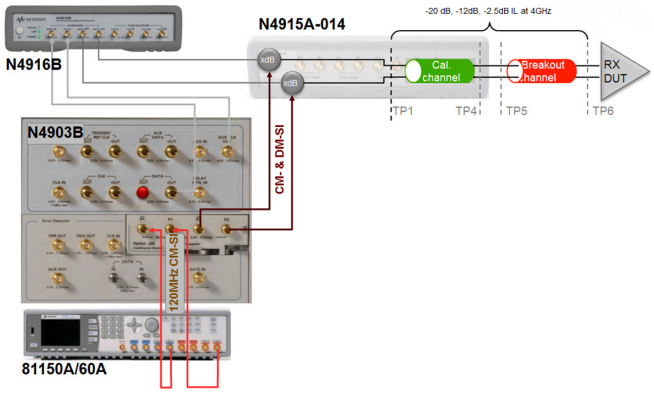


Figure 4.1-1. J-BERT N4903B based ASIC test setup for 8 GT/s. Signal path to DUT RX is shown only

The J-BERT M8020A offers built-in CM-SI and DM-SI at the same time removing the need for additional non ISI stressors.

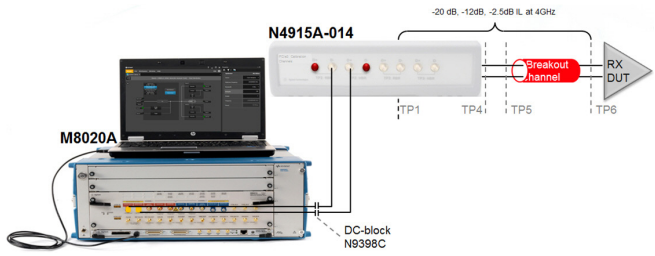


Figure 4.1-2. J-BERT M8020A based ASIC test setup for 8 GT/s. Signal path to DUT RX shown only

The J-BERT M8020A can provide a 100 MHz reference clock to the ASIC under test or run on a provided 100 MHz reference clock. The latter can be beneficial in case a disruption free reference clock needs to be maintained.

The base specification test setups for 2.5 GT/s and 5 GT/s based on the J-BERT M8020A are similar with the exception of the required ISI channel. In case an adjustable ISI trace or a switch matrix is used to select different fixed ISI traces a setup which can be used to test all transfer rates without reconnection can be achieved.

CEM specification

Receiver test setups for CEM / PHY Test Specification testing mostly differ from base specification setups in ISI channel and fixtures. ISI is included in the CEM compliant fixtures which can be acquired via the PCI-SIG and no additional ISI traces are required. The fixture for the 16 GT/s did not exist at release of this document.

Add-in card (AIC)

Unfortunately it is not possible to perform a RX test for all transfer rates using the same fixture. A gen2 CBB is required for 2.5 GT/s, 5 GT/s, and 8 GT/s short channel but a gen3 CBB is required for the mandatory long channel test for 8 GT/s.

The CEM AIC test setup based on J-BERT N4903B required a coupling of DM-SI into the data signal at the outputs of the N4916B De-emphasis signal converter.

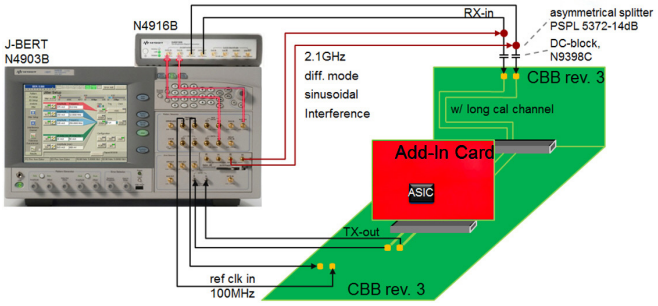


Figure 4.2.1-1. J-BERT N4903B based 8 GT/s AIC test setup

Because of the integration of TX EQ capabilities and DM-SI as well as CM-SI capabilities into the data outputs of J-BERT M8020A, external power coupling is no longer necessary.

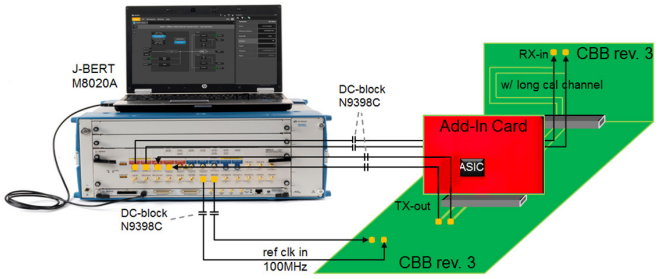


Figure 4.2.1-2: J-BERT M8020A based 8 GT/s AIC test setup

The only accessories the J-BERT M8020A CEM AIC setup requires are DC blocks in between the connections to the CBB and cables.

Mainboard (system)

A challenge when testing systems is the synchronization of the BERT to the system under test since it is not possible to force a system to run on a BERT provided reference clock. While the J-BERT N4903B has built-in clock multipliers, the very low loop bandwidth of the built-in PLL is not compatible to the CC architecture. An external clock multiplier, the N4880A, is required. Another problem can be the ISI on the data signal returned to the BERT error detector (ED). For AIC testing it is possible to keep the return path as short as possible. Systems that do not have a shorter break out for the BERT ED will have closed eyes especially on server mainboards. BERT EDs so far do not have built-in equalizers and therefore an external repeater can be required.

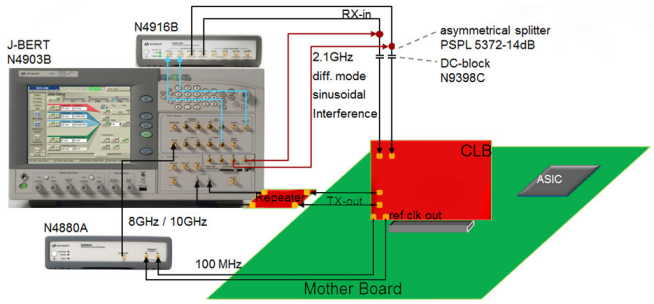


Figure 4.2.2-1. J-BERT N4903B system test setup

J-BERT M8020A has an integrated PCI Express compliant reference clock multiplier which can generate the necessary clock for the BERT from the system's 100 MHz reference clock. The multiplier's PLL is high enough to transfer SSC allowing testing of systems with SSC turned on. A built-in CTLE on each data input of the J-BERT M8020A allows testing of long traces on systems without the use of external repeaters.

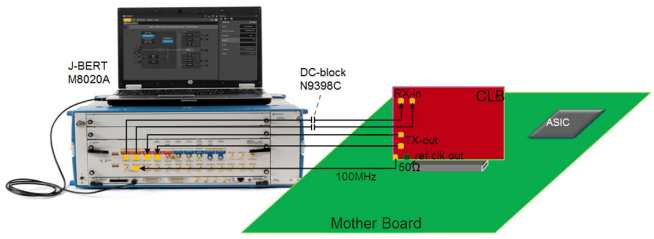


Figure 4.2.2-2. J-BERT M8020A based system test setup

A system test setup is now as simple as an AIC test setup.

Connection table

DC blocks required between J-BERT M8020A outputs and DUT inputs.

Connection	ASIC	AIC	System	Comment
M8020A Data Out → ISI channel → DUT RX	x	x	x	
DUT TX → M8020A Data In	x	x		Use M8020A built-in CDR
DUT TX → ISI channel → M8020A Data In			x	Use M8020A built-in CTLE if needed and CDR
M8020A Trigger Out → DUT 100 MHz Reference Clock In	(x)	x		ASIC: only if DUT needs to run on BERT reference clock; not the case for SRIS or SRNS
DUT 100 MHz Reference Clock Out → M8020A Reference Clock In	(x)		x	Use M8020A built-in reference clock multiplier ASIC: only if BERT needs to be synchronized to DUT reference clock; not the case for SRIS or SRNS

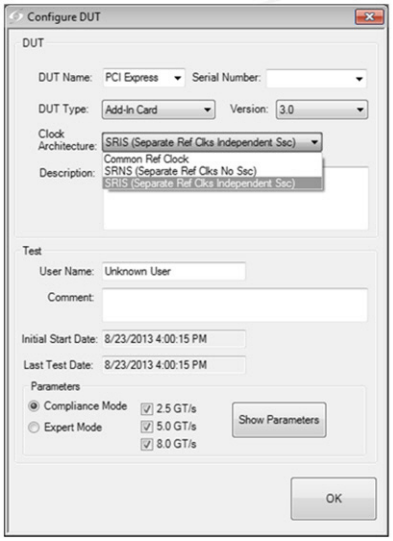
Summary test setups

De-emphasis output stages, reference clock multipliers, stressors, and CDR and CTLE for the BERT ED are all integrated into the J-BERT M8020A. This minimizes the necessary components for receiver test to the BERT itself, DC blocks, reference channel + test fixtures, and an oscilloscope for calibration.

Test Automation

Differences in specification reference points, specification and calibration methods for the transfer rates and between base and CEM / PHY Test Specification make receiver testing and especially the stress signal calibration a challenging task. Some of the calibration steps are tedious and take a long time. A test automation SW significantly reduces calibration errors and time an operator needs to attend a calibration or test.

Keysight's N5990A Test Automation Platform offers a complete PCI Express receiver test suite. It is the only test automation software covering all transfer rates, base specification as well as CEM / PHY test specification testing for AICs, and systems as well as clocking architectures including the new SRIS use case.



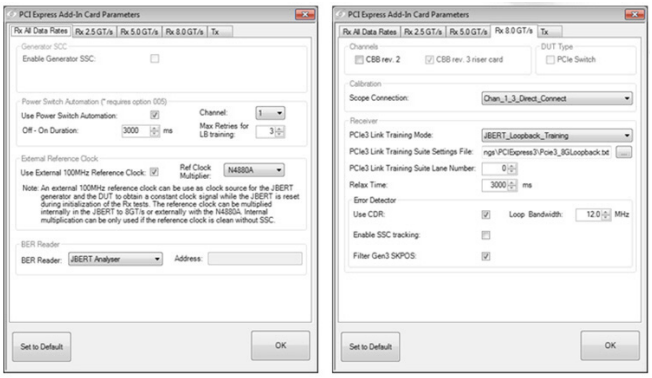


Figure 5-1. N5990A-101 PCI Express test automation SW covers all transfer rates, synchronous and asynchronous operation modes and device types

The implemented calibration procedures use the PCI-SIG SEASIM and SIGTEST when required. User interaction is required only when setup changes need to be performed.

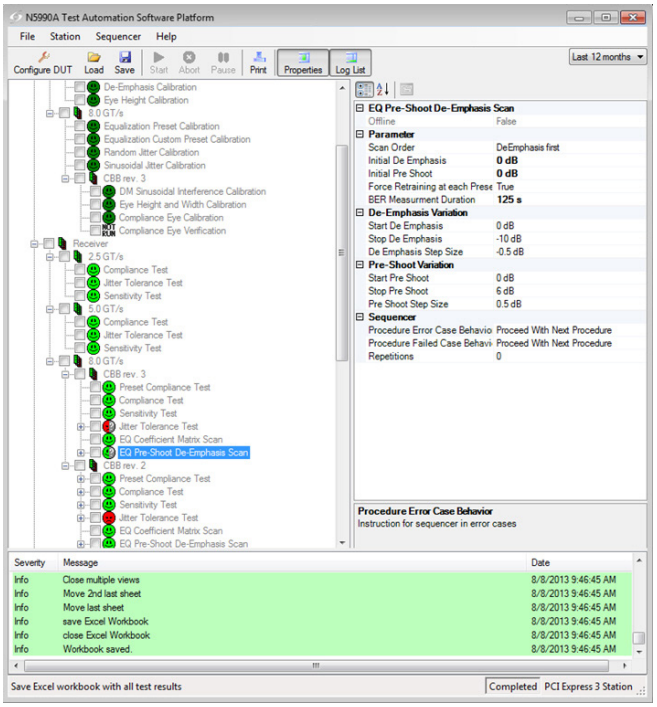


Figure 5-2. Calibration, compliance testing as well as characterization made easy with the N5990A-101 PCI Express Test Automation SW

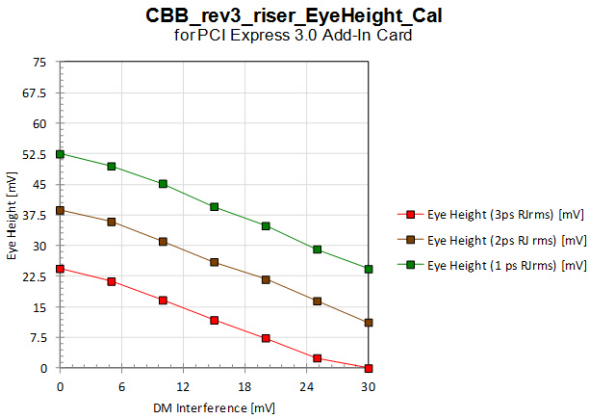
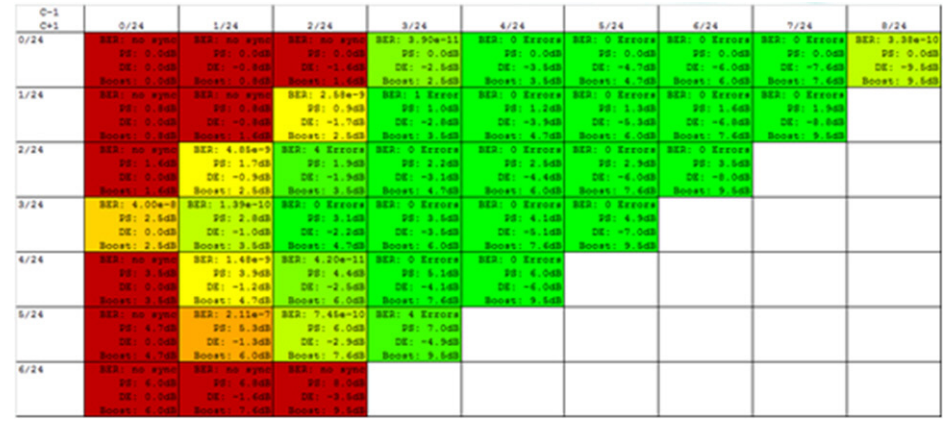


Figure 5-3. 8 GT/s eye height calibration for CEM AIC test – N5990A-101 controls entire setup including real time oscilloscope

Next to compliance testing the N5990A-101 PCI Express RX test suite offers extensive characterization tests like tolerance tests and sensitivity tests. Two different methods to determine the most suitable TX EQ combination for a DUT for 8 GT/s are included.



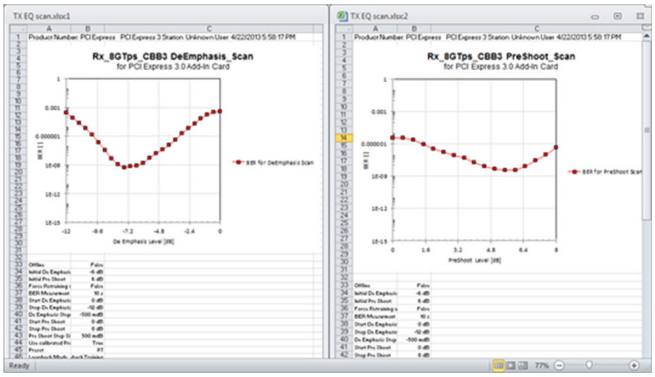


Figure 5-4. TX EQ matrix scan as well as a pre-shoot and de-emphasis scan are offered in the N5990A-101 to find best pre-shoot / de-emphasis combination for RX under test

Conclusion

The J-BERT M8020A High-Performance BERT is a scalable BERT system for computer bus as well as datacenter interface applications. The design of the J-BERT M8020A was oriented on the needs for receiver testing for PCI Express. The extension of stress sources, integration of de-emphasis into each pattern generator data output as well as equalizing capabilities into each error detector data input, and integrated reference clock multipliers simplify the PCI Express receiver test setups greatly compared to the test setups based on its predecessor J-BERT N4903B. The M8041A BERT module of the J-BERT M8020A BERT system offers data ranges up to 8.5 Gb/s or up to 16.2 Gb/s. The 16.2 Gb/s version allows testing of receivers for all four transfer rates. The J-BERT M8020A BERT will be supported by the N5990A Test Automation Platform for PCI Express. Planned enhancements of the J-BERT M8020A BERT system include support for a LTSSM enabling real handshaking for device loopback training through configuration and recovery. The J-BERT M8020A helps to master PCI Express receiver designs.

Recommended J-BERT M8020A Configuration for PCI Express Receiver Testing

J-BERT M8020A BERT

Product number	Description	Quantity	Comment
M8020A-BU1	AXIe Chassis 5 slot with embedded controller	1	Alternatively M8020A-BU2 plus external PC
M8070A-0TP	M8070A Software	1	Alternatively M8070A-0NP M8000 SW network license
M8041A-C16	BERT one channel, data rate up to 16.2 Gb/s	1	If testing up to 8 GT/s is desired only option M8041A-C08 can be used instead
M8041A-0G3	Advanced jitter sources, SSC for receiver characterization	1	Jitter sources
M8041A-0G7	Advanced interference sources for receiver characterization	1	Interference sources
M8041A-0G4	Multi-tap de-emphasis	1	Pre and post cursors for data output
M8041A-0S1	Interactive Link Training for PCI Express	1	M8020A handshaking for PCI Express, available summer 2014
M8041A-0S2	SER/FER analysis for coded and retimed loopback	1	SKP OS filtering for all transfer rates
M8041A-0G6	Reference clock input with multiplying PLL	(1)	Required only if M8020A needs to be synchronized to a 100 MHz clock, e.g. system test
M8041A-0A3	Analyzer equalization	(1)	Required only if a CTLE is needed at data inputs of M8020A, e.g. system test on long server mainboard lanes

Accessories

Product number	Description	Quantity	Comment
N9398C	DC block, 50 kHz to 26.5 GHz, 3.5 mm	4 to 6	4 in case of SRIS or M8020A is synchronized to provided 100 MHz reference clock 6 in case 100 MHz reference clock is provided by M8020A
M8041A-801	3.5 mm 0.85 m matched pair cables	2 to 4	Depends on test setup, see chapter 4
M8048A-001 M8048A-002 M8048A-801	Four shorter trace pairs Four longer trace pairs short SMA matched pair cables	(1) (1) (1)	Base specification testing only
CBB and CLBs		(x)	Required for CEM / PHY Test Specification testing only, CBBs and CLBs are available from the PCI-SIG

Test automation

Product number	Description	Quantity	Comment
N5990A-010	Test Flow Controller (Test Sequencer), GUI, Instrument Drivers, Report Generation	1	One license required per host computer, can be used with multiple application specific test libraries
N5990A-101	PCI Express Gen1 , Gen2 and Gen3 Receiver Tests with J-BERT	1	PCI Express Receiver Test library
N5990A-201	Interface to N5393C PCI Express TX Test Software (N5393C not included)	(1)	Optional, allows control of the Keysight RT-oscilloscope PCI Express TX compliance SW from the N5990A GUI
N5990A-001	Data Base and Web Browser Interface	(1)	Optional
N5990A-500	User Programming (API Including C-Sharp Templates), Additional Developer License	(1)	Optional
N5990A-301	PCI Express Link Training Suite	(1)	Recommended if M8041A-0S1 is not used

Related Literature

Publication title	Publication type	Publication number
PCI Express Revision 2.0 Receiver Testing	Application Note	5990-3233EN
Accurate Calibration of Receiver Stress Test Signals for PCI Express rev. 3.0 Assuring Interoperability at Data Rates of 8 GT/s	Application Note	5990-6599EN
How to Pass Receiver Test According to PCI Express 3.0 CEM Specification with Add-In Cards and Motherboards	Application Note	5990-9208EN
PCI Express Receiver Test 8 GT/s Method of Implementation		www.pcisig.com
Keysight J-BERT M8020A High-Performance BERT	Data Sheet	5991-3647EN
Keysight J-BERT N4903B High-Performance Serial BERT	Data Sheet	5990-3217EN
Keysight N5990A Test Automation Software Platform	Data Sheet	5989-5483EN
Keysight M8048A ISI Channels	Data Sheet	5991-3648EN

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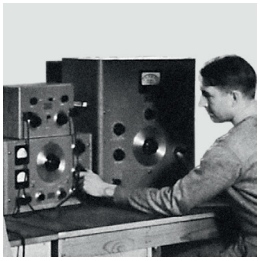

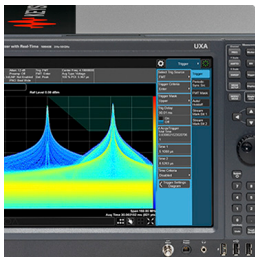

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