



# 116-Gbit/s PAM4 BERT for 400GbE/800GbE PAM4 ED MU196040B

Signal Quality Analyzer-R  
MP1900A Series



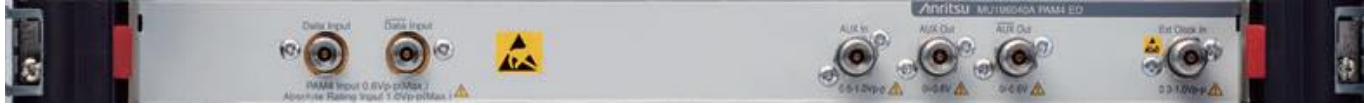
# Outline of 116-Gbit/s PAM4 Error Detector for 400GbE/800GbE

- **High-performance BERT for 116-Gbit/s PAM4 error-free measurement**  
Simplify previously difficult PAM4 error troubleshooting
- **Industry-best high input sensitivity of 36 mV EH@53.125 Gbaud**  
Support more accurate evaluations up to 116-Gbit/s PAM4.
- **All-in-one 58-Gbaud PAM4 receiver test solution with built-in Clock Recovery and Equalizer functions**  
Support faster testing and debugging with easy measurement system configuration
- Wideband operation: 2.4 Gbaud to 64.2 Gbaud for NRZ  
2.4 Gbaud to 58.2 Gbaud for PAM4
- Support CEI-112G-VSR Stressed Receiver Input Test
- Built-in 58-Gbaud PAM4 Clock Recovery
- PAM4 symbol Capture function
- Multichannel measurement (up to 4ch/unit)

Target Applications: 100/200/400/800GbE, CEI-112G-VSR

# 58-Gbaud PAM4 ED Specifications

## PAM4 ED MU196040B



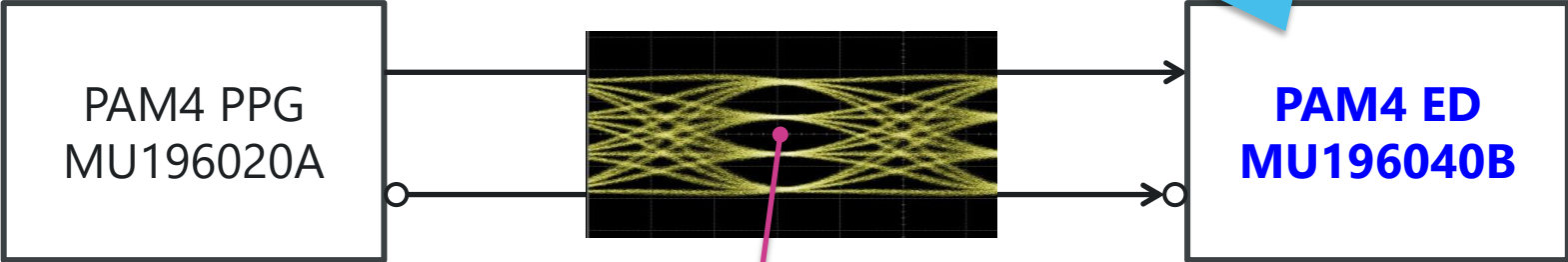
- Baud rate: 2.4 Gbaud to 58.2 Gbaud (PAM4)  
2.4 Gbaud to 64.2 Gbaud (NRZ)
- Input amplitude (max.): 1.0 Vp-p (NRZ, PAM4)
- Input sensitivity (typ., Eye Height): 36 mV at 53.125G  
23 mV at 26.5625G
- Built-in Clock Recovery (NRZ/PAM4):  
2.4 to 29 Gbaud or 32.1 Gbaud  
51 to 58.2 Gbaud (Extension option)
- Built-in Equalizer: DFE (1.4 dB) + Low-frequency Equalizer (2 dB)\*
- Analog bandwidth: >40 GHz (nominal)
- SER measurement, logic error analysis using Diagnostics Mode

\*Response at <1 GHz controlled by low-frequency Equalizer function

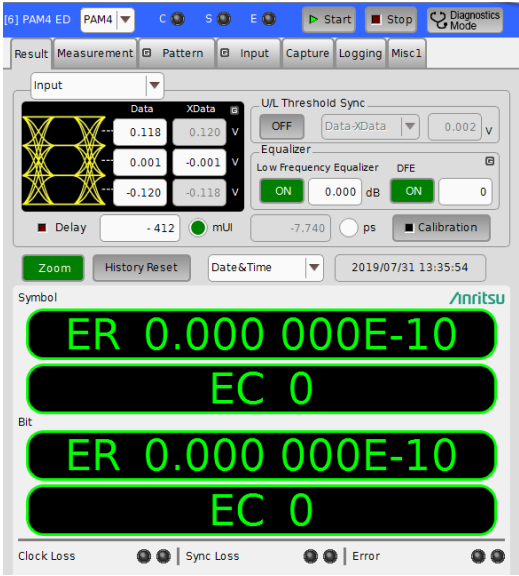
# Best Level High-Sensitivity Input Performance

High sensitivity input of 36 mV (typical at 53.125 Gbaud) simplifies previously difficult PAM4 error troubleshooting measurements.

**Error-Free** at 53.125 Gbaud  
Best level PAM4 sensitivity

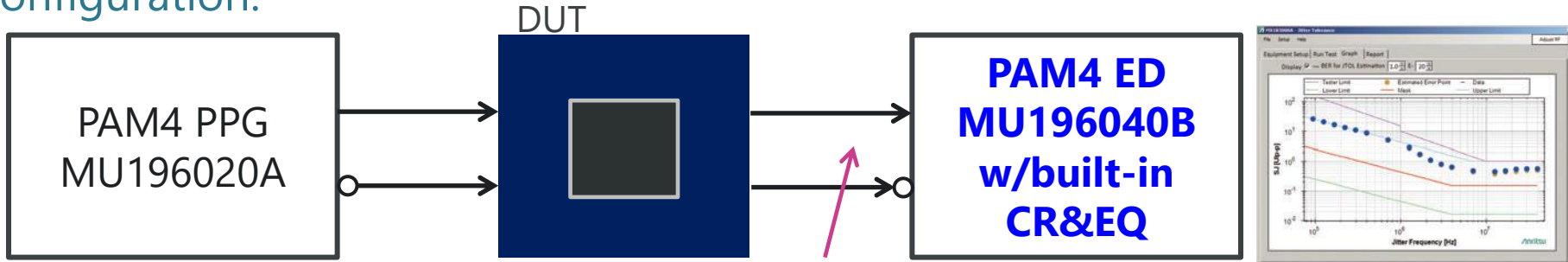


Typ. 36 mV EH/Eye



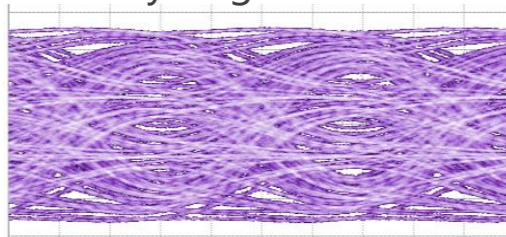
# All-in-One BERT w/ PAM4 Built-in Clock Recovery & Equalizer

Connections with external equipment and components are eliminated. PAM4 Jitter Tolerance measurements are simplified by the easy system configuration.



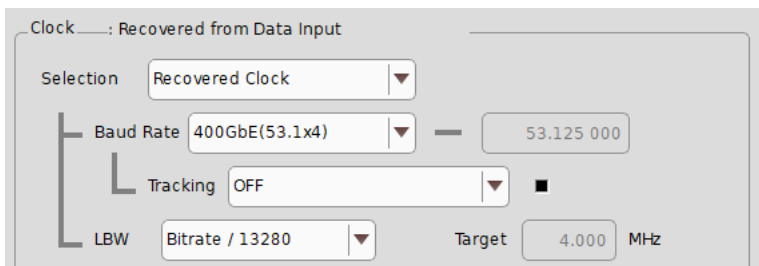
- Jitter
- ISI Control

Support BER measurement of closed-Eye signal with stress

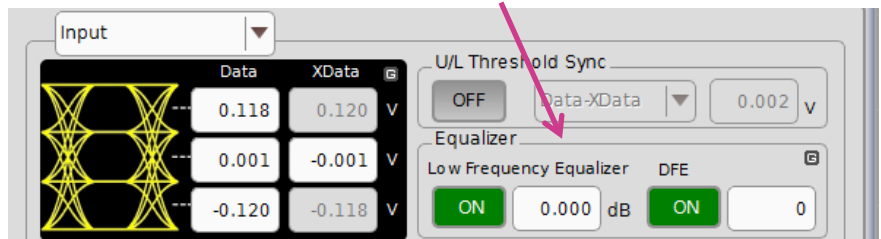


Support PAM4 Jitter Tolerance test

- Built-in Clock Recovery to re-time DUT signal for 58-Gbaud PAM4 JTOL testing



- Equalizer function to open Eye of VSR stressed signal for measuring BER



# CEI-112G-VSR Stressed Input Test Support

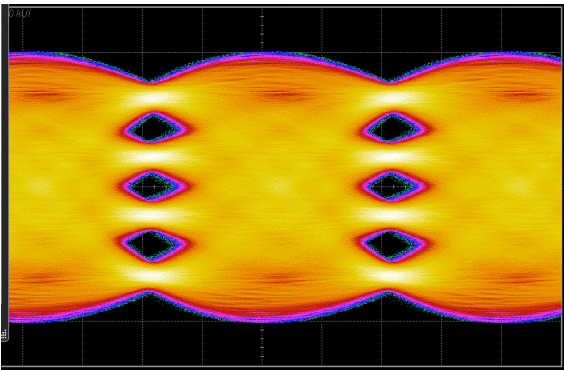
The true DUT low-error-rate Rx performance can be tested with added stress.

## CEI-112G-VSR Rx input specification

Item	Spec. (112G-VSR-PAM4)
Baud Rate	36 to 58 Gbaud
Channel Loss	12 dB at 26.5625 GHz
EH6	>37 mV
EW6	>0.2 UI (>3.76 ps)
Target BER	<E-6



Using MU196020A PPG output and ISI board as calibrated signal (oscilloscope CTLE 2.5 dB setting) supporting Rx Input standard performance

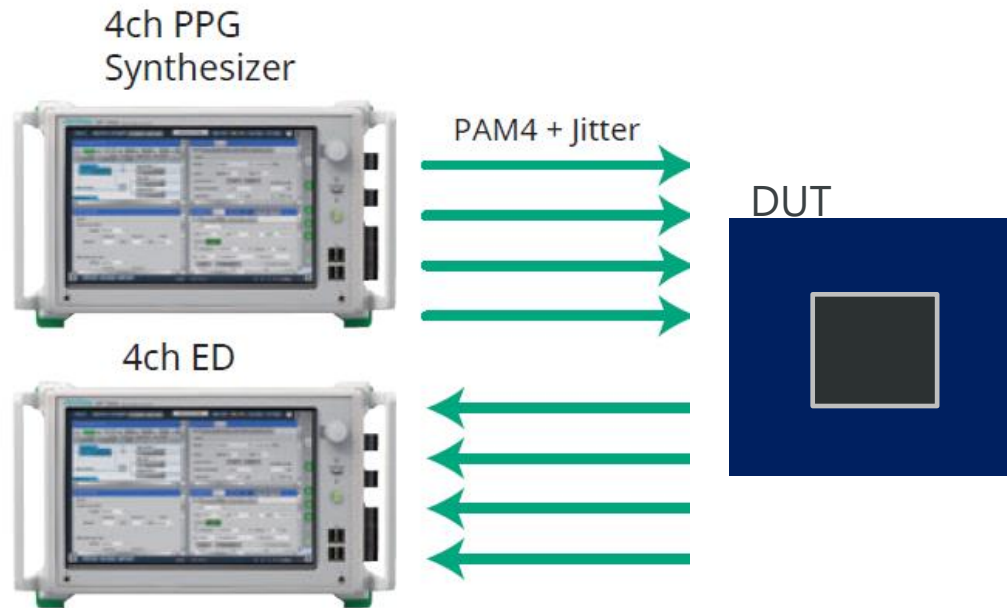


Higher sensitivity performance (E-8 or lower) than receiver model defined by CEI VSR standard (E-6)

**PAM4 ED  
MU196040B**

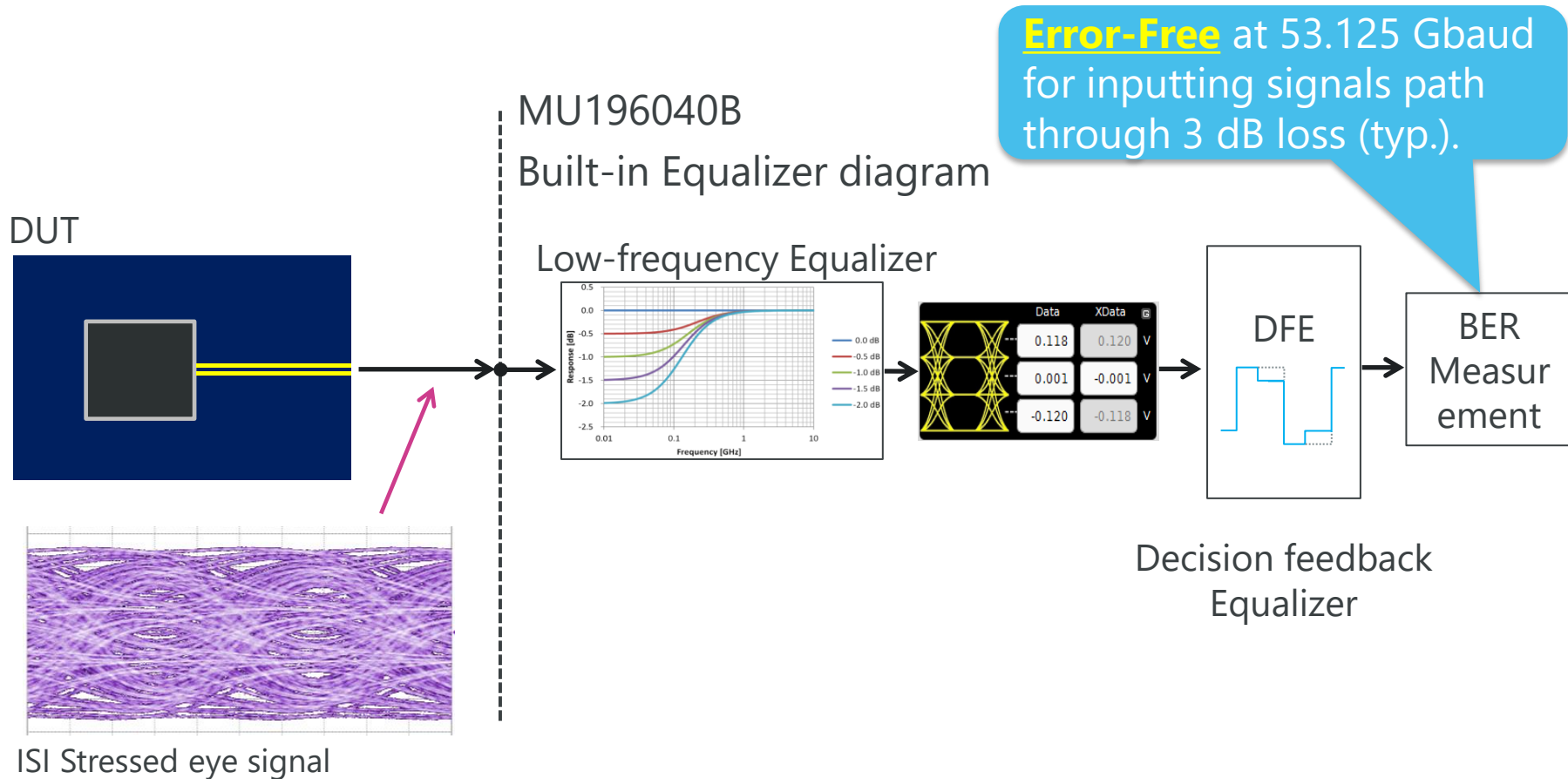
# Multichannel Measurement Support

- Use of two MP1900A units supports BER measurement for up to 4ch Tx and 4ch Rx, totaling 400 Gbit/s.
- The high module expandability helps cut future measuring equipment costs.



# Built-in Equalizer

Combination of built-in Equalizer function and high input sensitivity performance supports higher accuracy measurements.





# FEC Symbol Capture Function (1/2)

- High input sensitivity performance of 36 mV EH at 53 Gbaud plus FEC Symbol Capture function for Pre-FEC jitter tolerance evaluation and analysis of FEC uncorrectable errors
- FEC Symbol Error detection for IEEE802.3-defined RS-FEC Codeword length and FEC Symbol length standards
- Input signal capture at timing exceeding settable FEC Symbol error threshold (1 to 32 per step), and Input Pattern Analysis function for causes of errors exceeding the threshold

MP1900A PAM4 BERT



Jitter Stressed Signal



Test Board

RX  
TX

SERDES/  
Transceiver

Block	Block Length	Trigger Position	Viewer Mode	Notation	Format	Error
1	4194300	2094896	Bin(MSB/LSB)	Pattern		<input checked="" type="checkbox"/> MS <input checked="" type="checkbox"/> CM

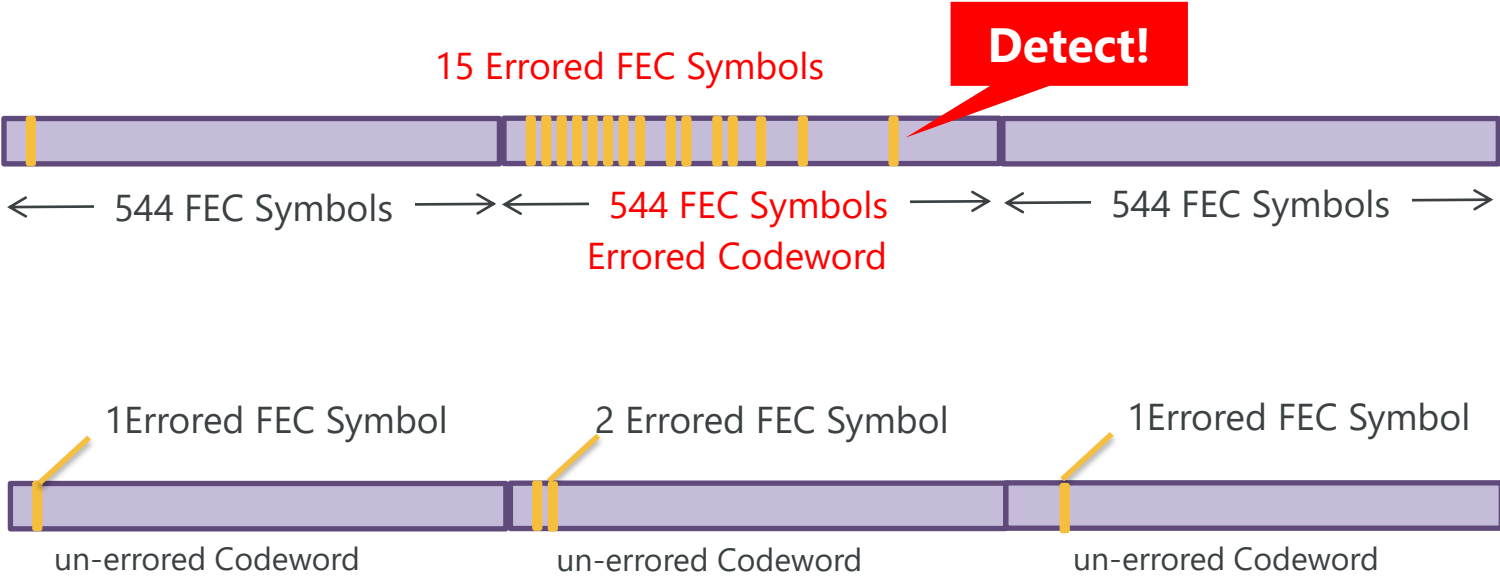
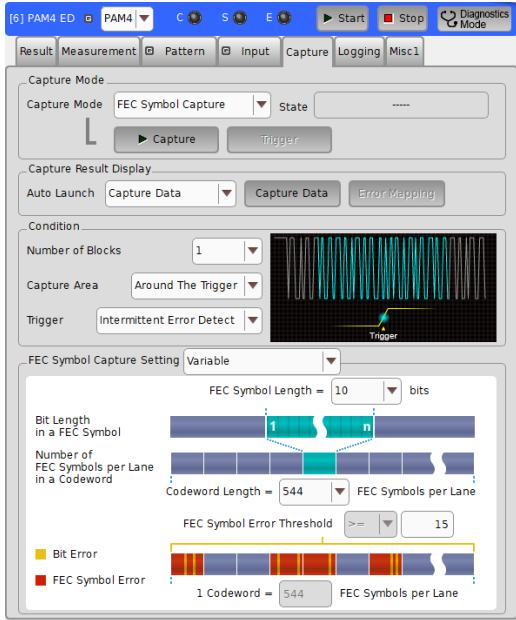
MSB	Block Address	Last Error Block Address	Total Error Counts	Total FEC Symbol Error Counts	Capture Depth
1	2097330	2097128	8	4194300	4194300
LSB	2096954	2097136	27	4194300	4194300

Capturing Detected FEC Symbols Errors

# FEC Symbol Capture Function (2/2)

Detect FEC Symbol Errors in Codeword.

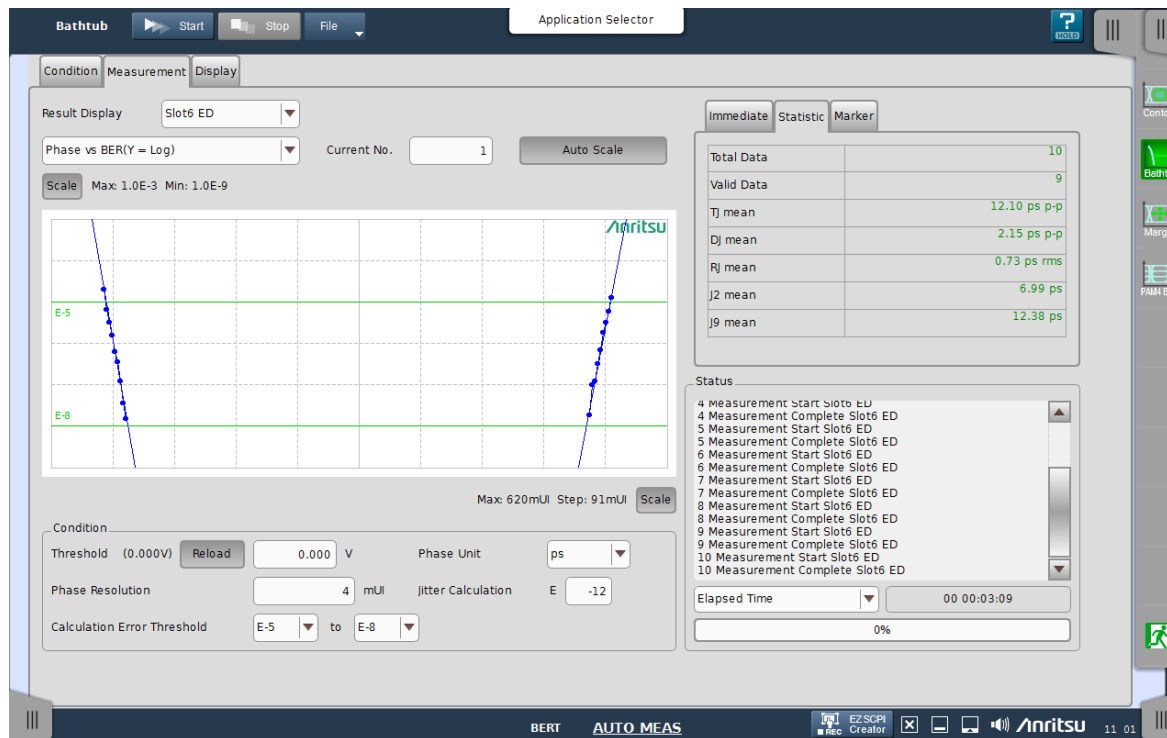
The input data is captured when the number of FEC symbol errors exceeds the threshold setting. The causes of FEC-uncorrectable errors can be analyzed from the captured data.



# Bathtub Jitter Analysis Function

The input signal jitter and phase margin can be measured automatically using the Bathtub function.

The wideband and high-sensitivity PAM4 ED helps more accurate measurement of DUT performance.



Example of PAM4 Signal Bathtub Measurement

# PAM4 Test Patterns (1/2)

Supports PAM4 test patterns specified by 200 and 400 GbE standards

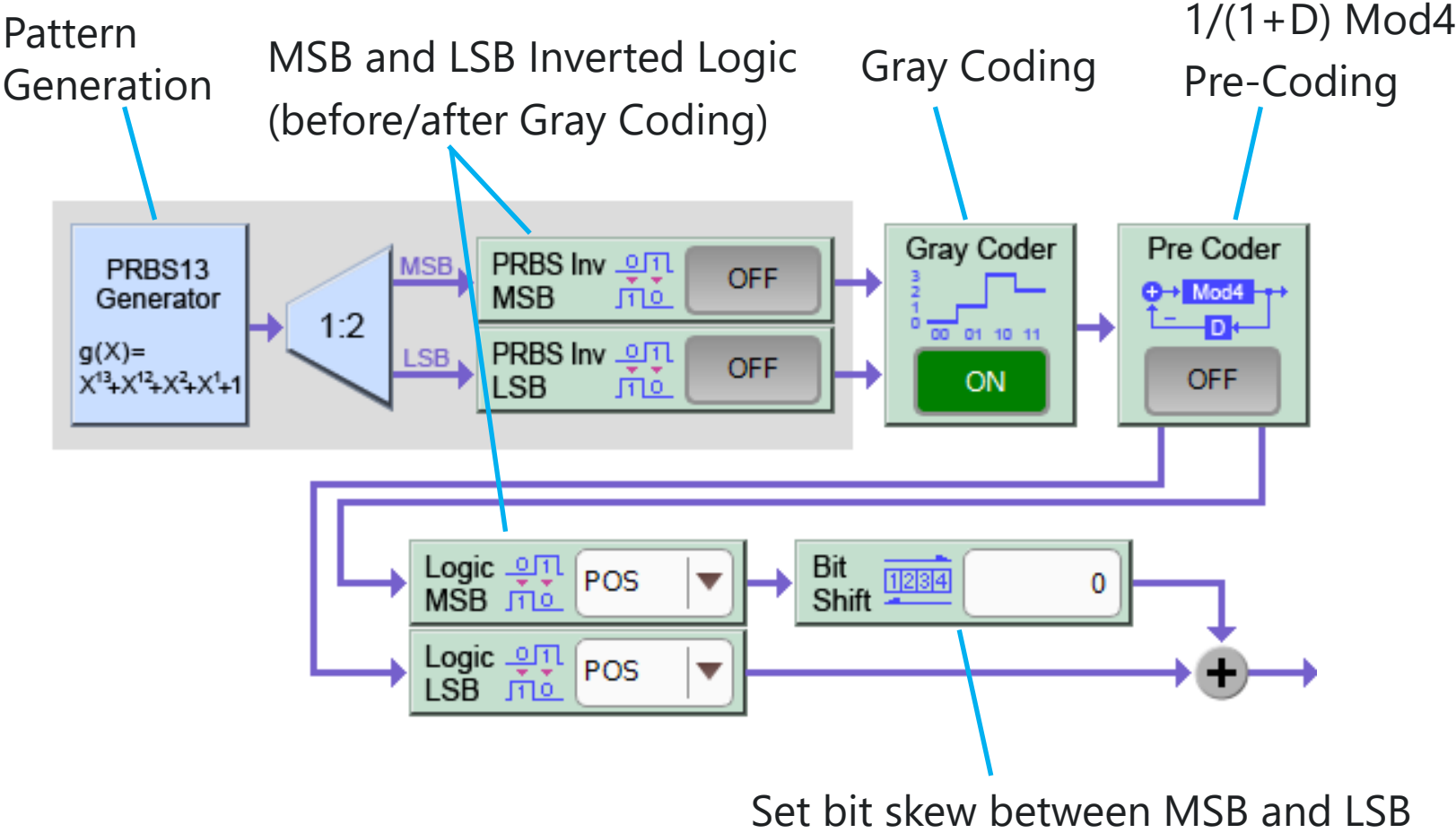
Supported Test Patterns	
CEI	QPRBS13-CEI, QPRBS31-CEI
IEEE	IEEE802.3bs/cd: PRBS13Q, PRBS31Q, SSPRQ, Square Wave IEEE802.3bj: QPRBS13, JP03A, JP03B, Transmitter Linearity
RS-FEC	RS-FEC Scrambled Idle 50G 1 Lane (26.5625 Gbaud, 50GBASE-KR/CR/SR/FR/LR) RS-FEC Scrambled Idle 100G 1 Lane (53.125 Gbaud, 100GBASE-DR) RS-FEC Scrambled Idle 100G 2 Lanes 26.5625 Gbaud, 100GBASE-KR2/CR2/SR2) RS-FEC Scrambled Idle 200G 4 Lanes (26.5625 Gbaud, 200GBASE-SR4/DR4/FR4/LR4) RS-FEC Scrambled Idle 400G 4 Lanes (53.125 Gbaud, 400GBASE-DR4) RS-FEC Scrambled Idle 400G 8 Lanes (26.5625 Gbaud, 400GBASE-FR8/LR8)
InfiniBand	PRBS13Q (InfiniBand), PRBS23Q, PRBS31Q(InfiniBand)
Fibre Channel	PRBS31Q (Fibre Channel)
General Purpose	PRBS7, 9, 10, 11, 13, 15, 20, 23, 31, Data (User defined) 4 to 256 Msymbol

Edit Data pattern using PAM4 symbol 0, 1, 2, and 3 values.

The screenshot shows the 'Pattern Editor' window. On the left, there is a list of memory addresses from 00000000 to 00000056. The first row (00000000) is highlighted with a dashed blue box and contains the values '3 2 1 0' at address +0, '0 1 2 3' at address +4, and a '3' at address +8. The rest of the row is empty. On the right, there are control fields: 'Number of Block' (empty), 'Row Length' (empty), 'Data Length' (set to 16), 'Number of Row' (empty), and 'Edit Block' (empty). At the bottom right, there are two dropdown menus: 'Viewer Mode' (set to 'Symbol(PAM4)') and 'Coding' (set to 'No Coding').

# PAM4 Test Patterns (2/2)

- BER measurement for different pattern generation methods depending on DSPs
- Efficient detection of pattern generation circuit differences as well as logic errors, such as inverted logic and bit skew



# Error Analysis Function (1/2)

Measurement of both symbol errors (MU196040B-041) and bit errors is useful for specifying error causes by comparing both measurement results. In addition, pressing [Details] offers more detailed analysis by confirming results for 12 types of errors.

Summary of error rates from the screenshot:

Symbol	Bit
ER: 2.834 100E-02	1.256 800E-04
EC: 116 708	143 642
%EFI: 50.000 000	
EI: 10	

PAM4 bit error measurement results

Separate error-rate measurements for MSB and LSB

Simultaneous measurement of 12 error types

MSB and LSB Error Rates:

	Total	INS	OMI
MSB ER	7.685 700E-05	1.857 800E-04	6.017 900E-07
MSB EC	82 942	82 560	382
LSB ER	9.531 300E-04	2.564 100E-05	1.499 000E-03
LSB EC	60 700	605	60 095

EC Error Breakdown by Level:

	Level 0	Level 1	Level 2	Level 3	Symbol
EC to Level 3	5 768	786	435		
EC to Level 2	6 445	9 467		6 447	
EC to Level 1	345		76 008	778	
EC to Level 0		8 987	786	456	
EC Total	12 558	19 240	77 229	7 681	116 708
ER Total	1.239 800E-02	1.887 100E-02	7.167 000E-02	7.620 700E-03	2.834 100E-02

# Error Analysis Function (2/2)

The Diagnostics Mode is useful for troubleshooting logic errors, such as inverted logic and MSB/LSB bit skew, etc. When these types of logic errors prevent synchronization, the cause can be determined using the separate MSB and LSB error results and the bit skew result between MSB and LSB.

The screenshot shows the Anritsu diagnostic interface. At the top, there is a 'Diagnostics Mode' button highlighted with a pink box. Below it, there are tabs for 'Result', 'Measurement', 'Pattern', 'Input', 'Capture', and 'Misc1'. The 'Input' tab is selected, showing eye diagrams and threshold settings. The 'U/L Threshold Sync' is set to 'ON'. Below the eye diagrams, there are controls for 'Delay' (0), 'mUI' (0.000), and 'ps' (0.000). A 'Calibration' button is also present. The 'History Reset' button and 'Date&Time' (2018/10/20 18:42:32) are also visible.

	Total	INS	OMI	Sync Loss
MSB ER	7.685 700E-05	1.857 800E-04	6.017 900E-07	345
MSB EC	82 942	82 560	382	
LSB ER	9.531 300E-04	2.564 100E-05	1.499 000E-03	456
LSB EC	60 700	605	60 095	
MSB + LSB ER	1.256 800E-04	1.777 000E-04	8.961 400E-05	777
MSB + LSB EC	143 642	83 165	60 477	

Below the table, there are fields for 'Clock Loss' (123), 'Frequency(kHz)' (32 000), and 'MSB/LSB Diff' (-10). At the bottom, there are fields for 'Clock Count' (MSB: 1.079 100E+09, LSB: 6.368 400E+07, MSB + LSB: 1.142 800E+09) and 'Middle Data Threshold' and 'Middle XData Threshold'.

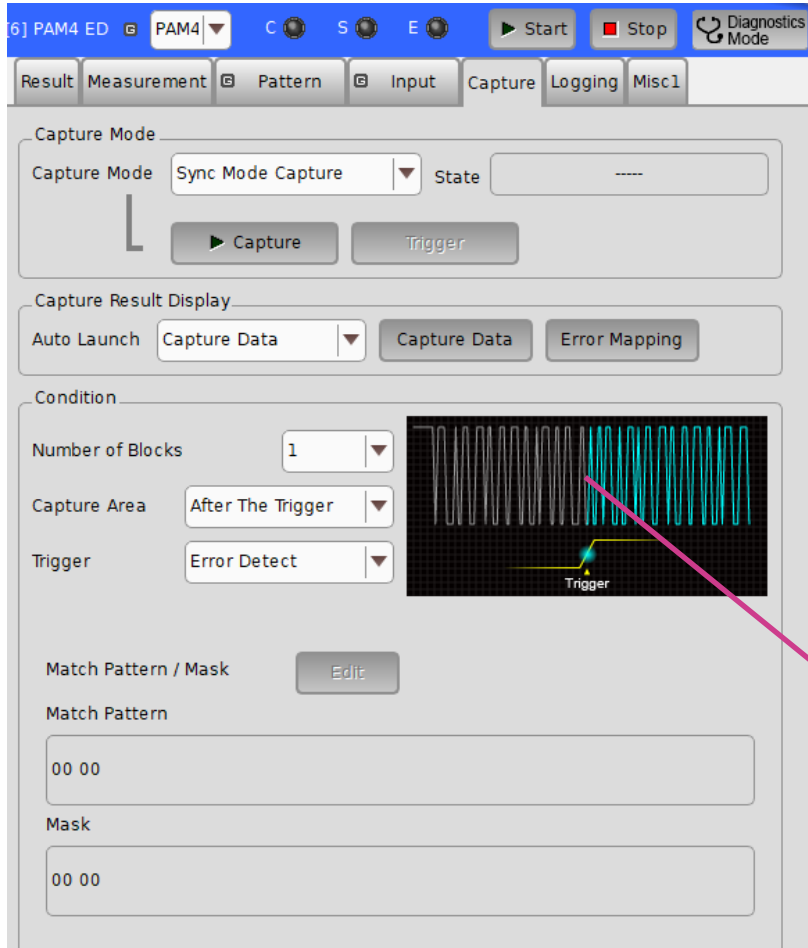
[Diagnostics Mode] button

Separate MSB and LSB error results

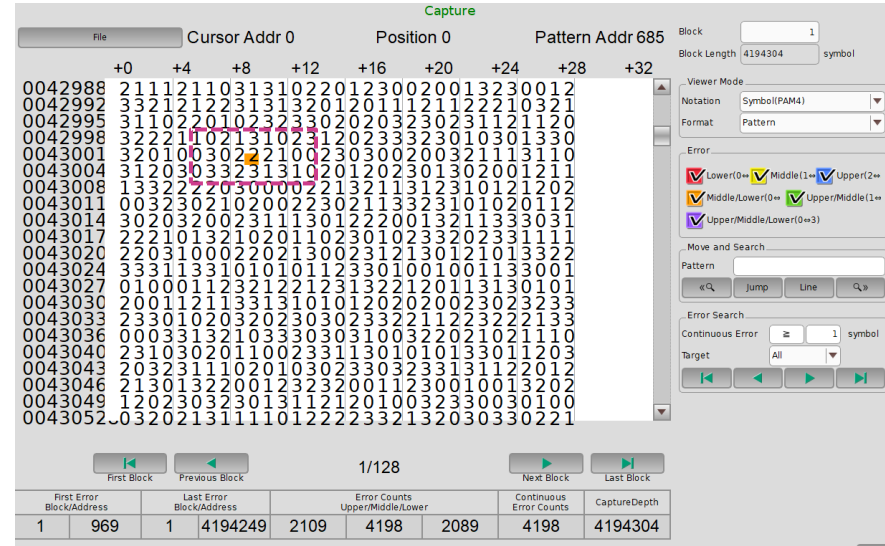
MSB/LSB bit skew detection

# PAM4 Symbol Capture Function

Capture function supports identification of PAM4 error symbols and cuts verification time.



Can specify error symbol position and level change of captured signal

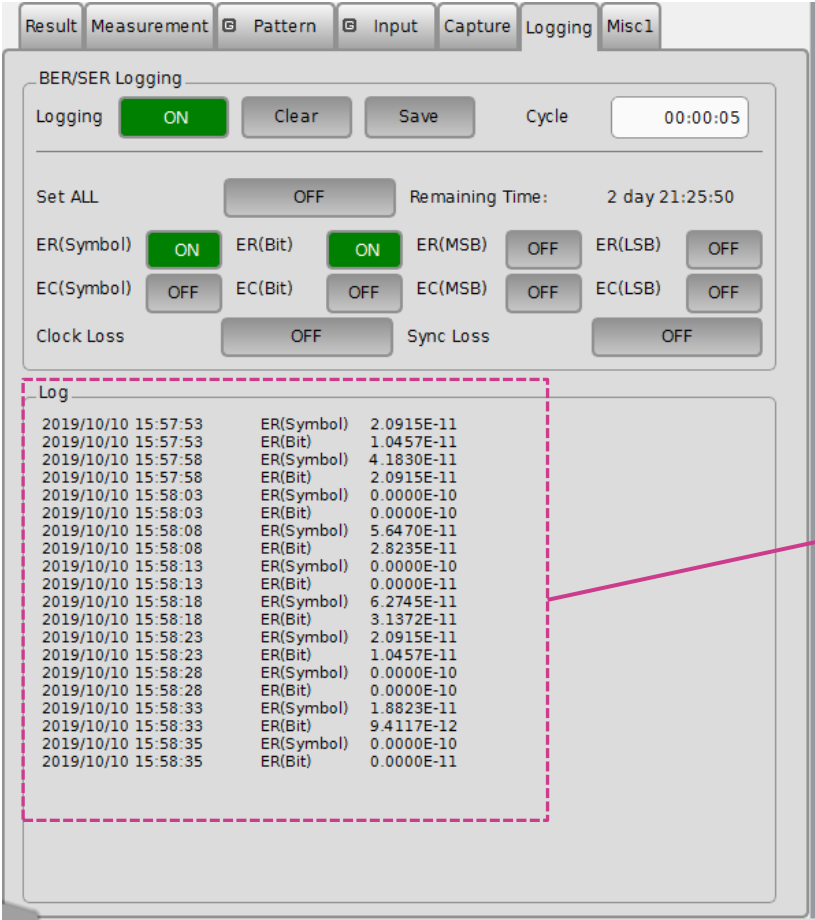


Start capturing inputting symbols using Error detection, Match pattern, or External trigger.



# Measurement Result Logging Function

Periodic saving of BER/SER, etc., measurement results can evaluate changes and stability of DUT time-dependent performance.



Sets measurement cycle and starts logging  
Saves results to file

Measurement item selection

Times-periodically saved measurement results

# Typical 58G PPG/ED Configuration

Model	Name	Option	Qty	Remark
MP1900A	Signal Quality Analyzer-R	-	1	
MU181000B	12.5GHz 4port Synthesizer	-	1	
MU181500B	Jitter Modulation Source	-	1	For jitter injection
MU196020A	PAM4 PPG	002, 011, 040, 042	1	
MU196040B	PAM4 ED	002, 011, 021, 023, 041	1	

## Options

Model	Name
MU196040B	PAM4 ED
MU196040B-001	32G baud
MU196040B-002	58G baud (max. 64.2 Gbit/s NRZ/58.2 Gbaud PAM4)
MU196040B-011	Equalizer
MU196040B-021	29G Clock Recovery (2.4 to 29 Gbaud)
MU196040B-022	32G Clock Recovery (2.4 to 32.1 Gbaud)
MU196040B-023	58G Clock Recovery Extension (51 to 58 Gbaud)
MU196040B-041	SER Measurement

Model	Name
MU196020A	PAM4 PPG
MU196020A-001	32G baud
MU196020A-002	58G baud
MU196020A-003	64G baud
MU196020A-011	4Tap Emphasis
MU196020A-030	Data Delay
MU196020A-040	Adjustable ISI
MU196020A-042	FEC Pattern Generation
MU196020A-050	Intel-Module Synchronization

# Appendix

# MP1900A New PAM4 BERT Features

- All-in-one, high-reproducibility, easily configured test solution
- High-quality waveforms for more accurate measurement
- Easy, low-cost, future-proof expandability supporting high bit rates and multichannels

## PAM4 One Box Test Solution



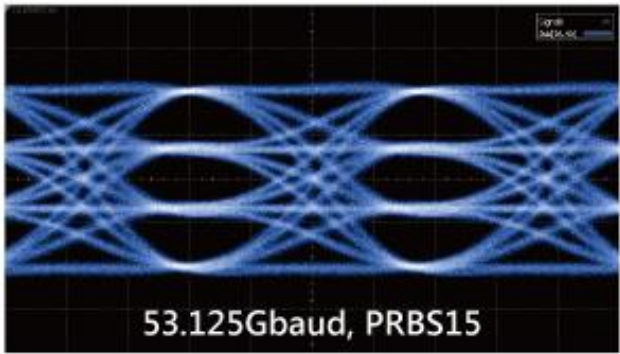
Emphasis 4Tap, 20dB

Built-in Clock Recovery

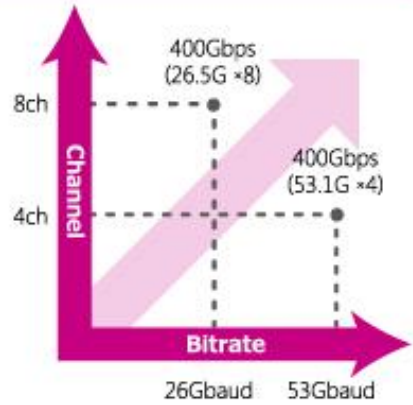
Jitter/Noise Addition

Jitter Tolerance Test

## Highest Level Waveform Quality

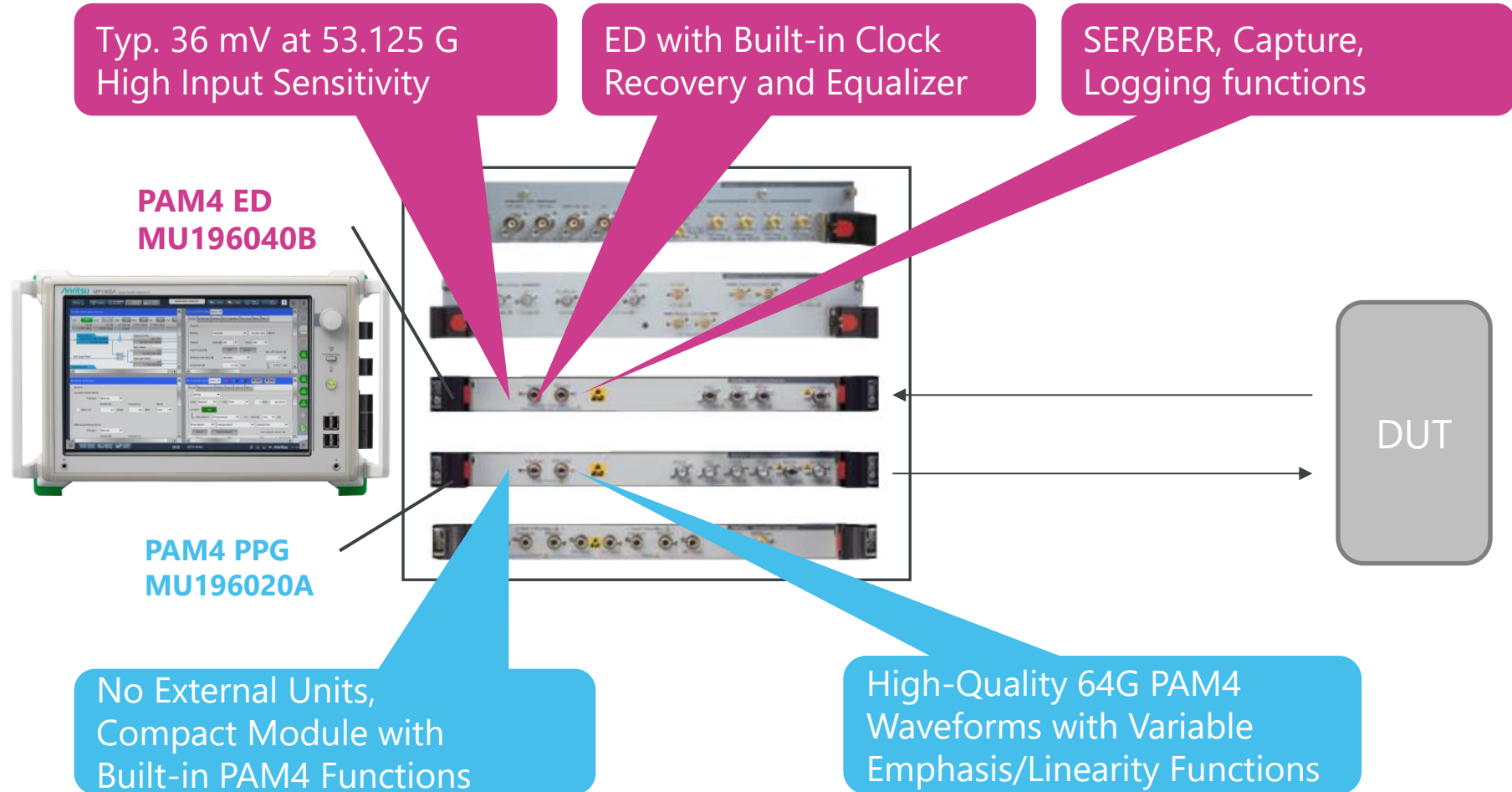


## Next-Generation Terabit



# All-in-One PAM4 BERT Solution

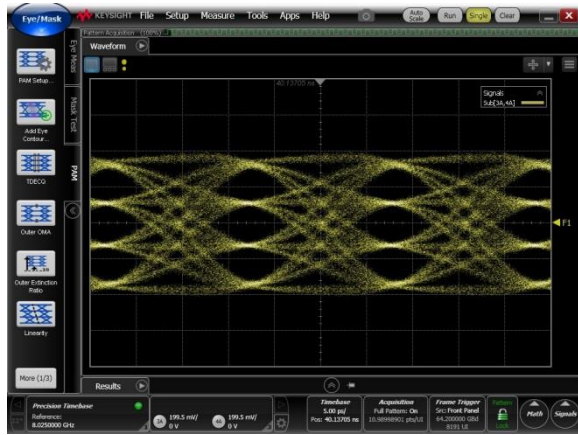
Easy-to-use and configure all-in-one solution with high reproducibility, helping cut test times



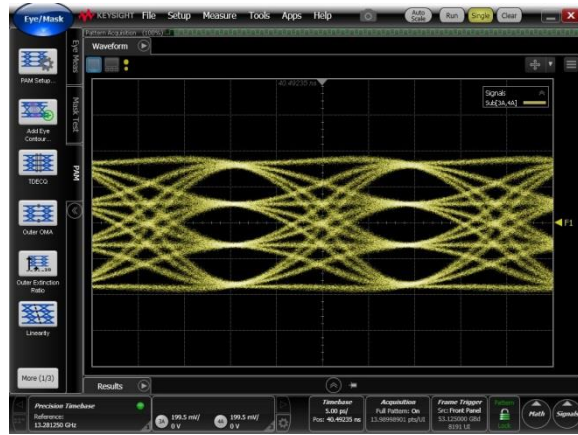
# High-Quality Waveform PAM4 PPG MU196020A

Best-in-class waveform quality with low Intrinsic Jitter (typ. 170 fs (rms)) and fast Tr/Tf (typ. 8.5 ps) for more accurate evaluation of actual DUT performance.

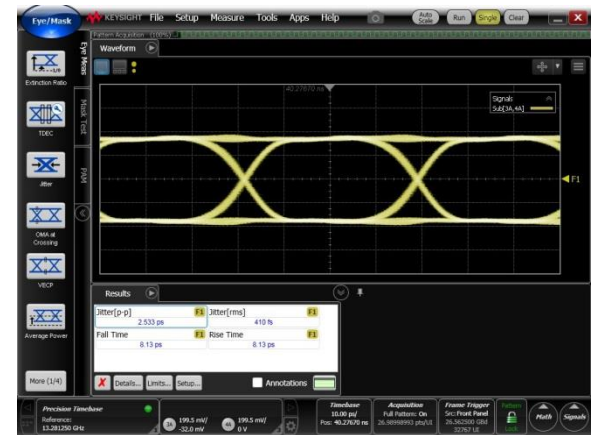
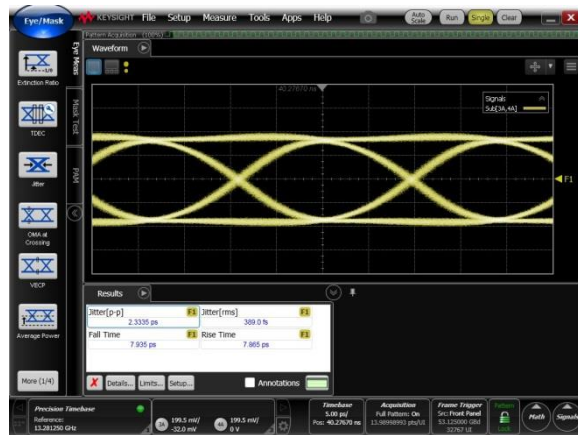
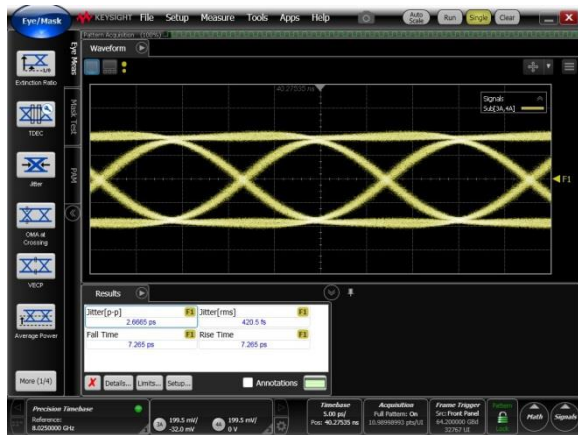
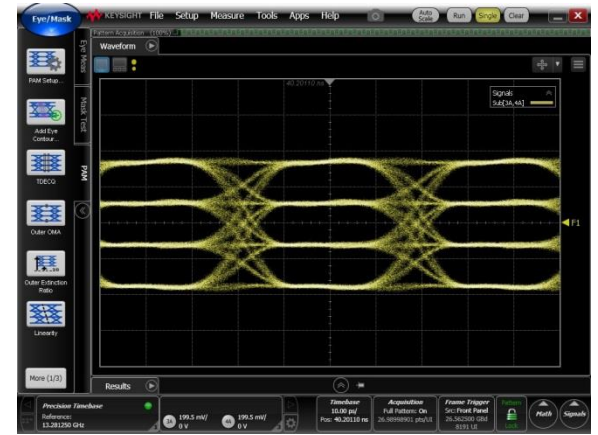
64.2 Gbaud



53.125 Gbaud



26.5625 Gbaud



Differential 1.4 Vp-p, PRBS13Q pattern, J1789A 40 cm cable + 70 GHz Scope

# PAM4 PPG MU196020A Specifications

Item	Specification
Operation Rate (PAM4/NRZ)	2.4 Gbaud to 32.1/58.2/64.2 Gbaud (option selection)
No. of Channels	1
Output Amplitude	70 mVp-p to 800 mVp-p (Single-end) 140 mVp-p to 1600 mVp-p (Differential)
Offset	-2 to +3.3 V
Emphasis	4 Tap, -20 to +20 dB
Channel Emulator	Generates waveform with insertion loss and simulates waveform with corrected insertion loss Set by loading S-Parameter file (S2P, S4P)
ISI	Simulates ISI generation waveform Set using loss (-8.00 to 8.00 dB) at CEI-specified Nyquist frequency Used in combination with channel board, such as J1800A/J1758A (optional accessories parts), or Noise Module MU195050A
Independently Variable PAM4 3 Eye	20% to 50% (PAM4 Amplitude 0/3 level = 100%)
PAM4 Pattern	SSPRQ, PRBS13Q, PRBS31Q, RS-FEC, etc.
PAM4 Pattern Error Addition	MSB Error, LSB Error, LSB&MSB Error, RS-FEC Symbol Error
Tr/Tf (20% to 80%)	8.5 ps (typ., NRZ)
Random Jitter	170 fs rms (typ., NRZ)
I/O Connector	V (f)
Jitter Addition Function	SJ, RJ, BUJ, SSC (with MU181500B)
Noise Addition Function	CMI, DMI, White Noise (with MU195050A (32.1G max.) and J1792A)

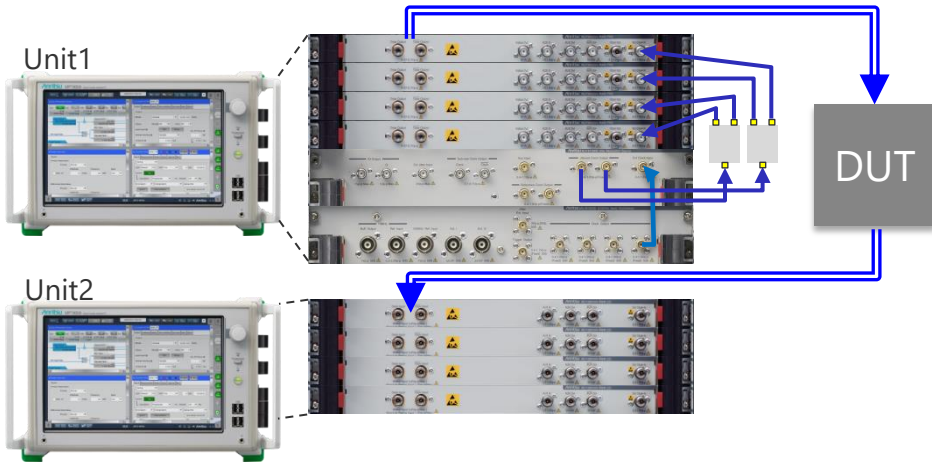


# PAM4 ED MU196040B Specifications

Item	Specification	Remarks
Baud rate	2.4 to 32.1 Gbaud/64.2 Gbaud (NRZ) 2.4 to 32.1 Gbaud/58.2 Gbaud (PAM4)	Select upper limit as option
Input Signal Method	NRZ, PAM4	
Number of Inputs	2 (Data, xData)	
Input Amplitude	1.0 Vp-p (max.)	
Input Sensitivity	36 mV (typ. at 53.125 G), 23 mV (typ. at 26.5625 G)	Eye Height of each PAM4 Eye
Stressed Margin	BER < 1 E-8	When inputting minimum eye signal defined in CEI-112G-VSR
Analog Band	>40 GHz (nominal)	
Clock Recovery Operation Range	2.4 to 29 Gbaud or 2.4 to 32.1 Gbaud 51 to 58.2 Gbaud Extension	Option
Equalizer	DFE (1.4 dB) + Low-frequency-Equalizer (2 dB)	
BER/SER Measurement	Total BER, MSB/LSB BER, SER (option) Logging, Capture (8 M bits/4 M PAM4 symbols)	
Patterns	PRBS, Data (max. 268 Mbit (symbol)), PAM4 Pattern (PRBS13Q, PRBS31Q, SSPRQ, QPRBS13-CEI, QPRBS31-CEI), Gray Code/PAM4 Pre-Code	
Connector	V (f)	



# Typical 100G x 4 Multichannel Configuration



## Unit 1

Model	Name	Qty
MP1900A	Signal Quality Analyzer-R	1
MU181000B	12.5 GHz 4 port Synthesizer	1
MU181500B	Jitter Modulation Source	1
MU196020A	PAM4 PPG (Opt-002, 011, 030, 040, 042, 050)	4
J1748A	Power Splitter (1.5 to 18 GHz)	2
J1728A	Electrical Length Specified Coaxial Cable (0.4 m, K-connector)	6

## Unit 2

Model	Name	Qty
MP1900A	Signal Quality Analyzer-R	1
MU196040B	PAM4 ED (Opt-002, 011, 021, 023, 040)	4

## Test Cable

Model	Name	Qty
J1789A or J1790A	Electrical Length Specified cable 0.4m or 0.8 m (V connector)	16

