Keysight N4880A
Reference Clock Multiplier

Achieve Accurate and Simplified Receiver Test for PCI Express®, SD UHS-II Host and MIPI® M-PHY® Devices

Data Sheet

- Multiply reference clocks from 19.2 to 100 MHz to provide external clock signals for J-BERT and ParBERT
- Preserve 33 kHz spread-spectrum clocking on reference clocks with multiplying PLL with 2 or 5 MHz loop bandwidth
- Detect small input signals with 100 mVpp sensitivity differential
- Utilize easy operation and remote control through USB connection and standalone GUI

KEYSIGHT TECHNOLOGIES

Verify the Performance of Next-Generation Receivers

The N4880A reference clock multiplier fills a critical requirement for R&D and test engineers who need to characterize and release the next generation of PCI Express main boards, MIPI M-PHY chipsets and SD card UHS-II host devices. With support for multiple reference-clock rates, the multiplier will help you accurately characterize and verify standard compliance under easy-to-reproduce test conditions.

Lock the Stressed-Pattern Generator to the System Reference Clock

In common reference-clock architectures, where the host cannot be driven by an external reference clock, it is necessary to lock the stressed-pattern generator to the same system reference clock used by the receiver under test. Locking the pattern generator to the receiver's reference clock ensures accurate and reproducible jitter-tolerance test results.

Work with Existing and Emerging Standards

This type of clocking architecture is required by several existing and emerging standards that use an architecture based on a common reference clock:

- PCI Express common reference clock architecture: test of main boards according to the PCI-SIG® card electromechanical specification (CEM)
- MIPI M-PHY: draft specification from the MIPI alliance. Here the N4880A multiplies a low-speed jittered clock from a signal generator to a higher rate jittered clock that can be used directly as the external clock signal for a BERT pattern generator
- SD UHS-II: draft SD card specification for host devices

Choose from Multiple Clock Rates

The N4880A reference clock multiplier supports all these standards.

The N4880A provides a multiplying phase-locked loop (PLL) with a 2 or 5 MHz loop bandwidth. The PLL lets you lock the pattern generator in a Keysight Technologies, Inc. J-BERT N4903B or ParBERT 81250A to the reference clock from the system under test. You can use the N4880A to multiply to the target data rate directly or you can use clock dividers of the pattern generators. The N4880A enables using J-BERT with its built-in SJ and SSC modulation sources by providing an external clock signal > 6.75 GHz. At its reference clock input, the N4880A supports the following clock rates:

- 100 MHz for PCIe® 1.x, 2.x and 3.0 testing
- 19.2, 26, 38.4 and 52 MHz for MIPI M-PHY devices
- 26 to 52 MHz for SD UHS-II host devices

The bandwidth of the multiplying PLL automatically adapts to the actual clock rate.

Easily Control all Settings

You can control the settings of the N4880A from a stand-alone software running on a Windows PC that is connected to the N4880A with a USB cable.

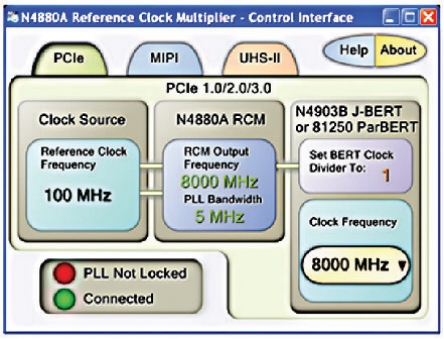

Figure 1. The Windows-based graphical user inter-face is used to control and monitor the N4880A.

Supports Multiple Applications

The N4880A can be used in a variety of applications. The following examples present typical use cases for PCI Express, SD card UHS-II and MIPI M-PHY receiver testing.

Application Example: PCI Express

When evaluating receiver performance of PCI Express main boards, one of the key challenges is the locking of the pattern generator to the system's reference clock: Most main boards cannot run on an external 100 MHz reference clock from a pattern generator.

With the N4880A, you can lock, for example, the J-BERT N4903B pattern generator to the 100 MHz PCIe reference clock. To enable locking, the J-BERT pattern generator must be set to its "external clock" mode. The clock input is driven by the N4880A reference clock multiplier phase-locked loop (PLL), which converts the 100 MHz reference clock into an 8 GHz clock (for PCIe 3.0) for J-BERT's external clock input. The N4880A does this while conserving all in-band jitter according to the PCIe specification, especially spread-spectrum clocking (SSC).

The recommended receiver test setup is shown in Figure 2. To achieve the required eye-height and eye-width stress conditions, this setup includes three-tap de-emphasis conversion by the N4916B, J-BERT's internal jitter sources and differential-mode sinusoidal interference. To support bit rates of 2.5 and 5.0 GT/s for PCIe 1.x and 2.x, the N4880A can be used as well in combination with J-BERT's external clock dividers of 4 and 2.

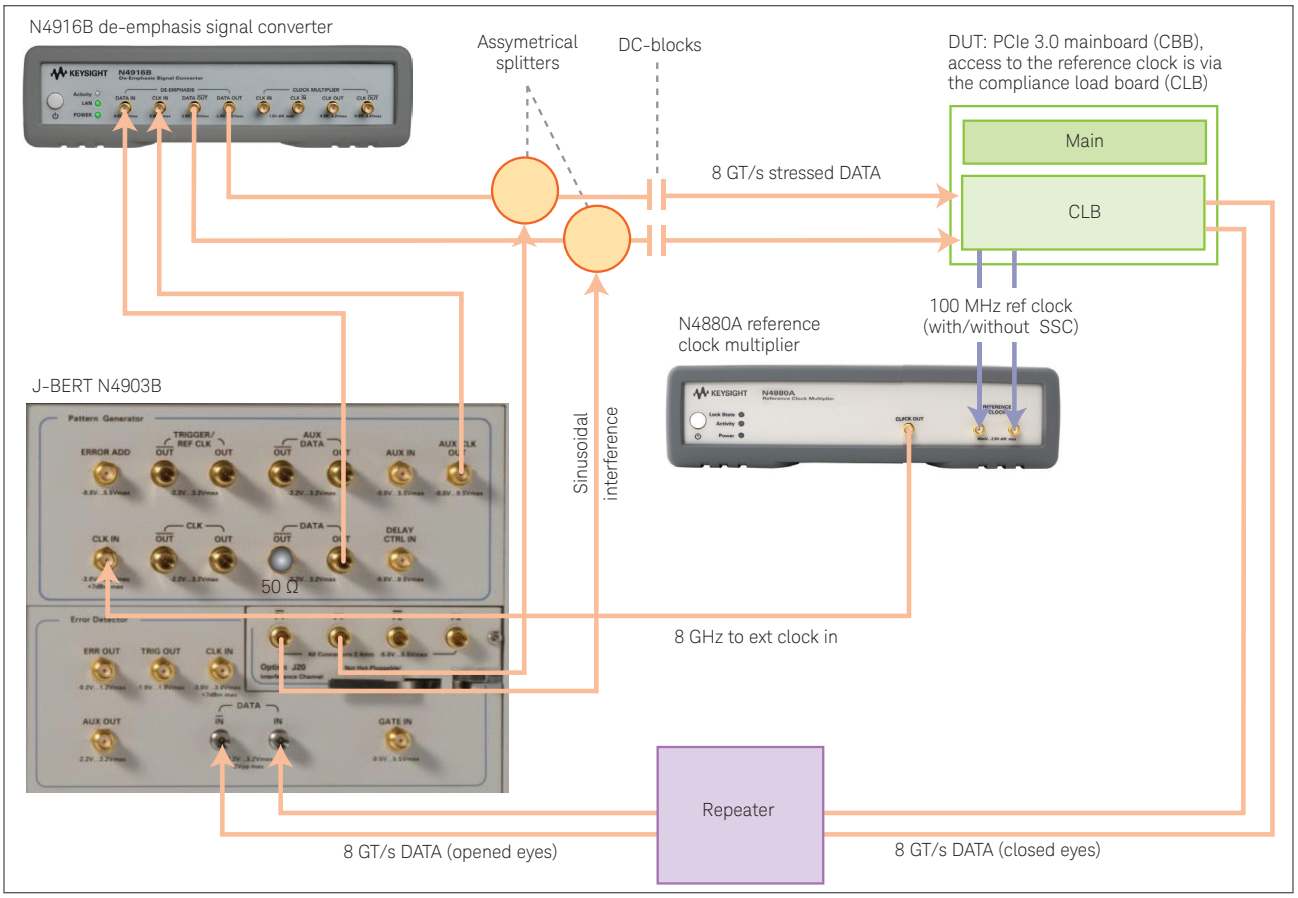

Figure 2. When testing PCIe 3.0 main boards, the N4880A reference clock multiplier is used to lock the J-BERT pattern generator and the de-emphasis signal converter to the 100 MHz reference clock from the board-under-test.

Application Example: SD Card UHS-II

UHS-II host receivers operate at bit rates between 390 and 1560 Mb/s. It is necessary to lock the stressed-pattern generator to the same reference clock as the host. UHS-II reference clocks operate from 26 to 52 MHz, have low voltage levels, provide slow transition times, and can carry huge amounts of SSC.

The N4880A has sufficient loop bandwidth to be transparent to SSC on the reference clock. Its excellent input sensitivity makes the N4880A capable of handling low voltage levels.

In SD card applications, the N4880A converts the UHS-II reference signal to a multi-gigabit external clock signal compatible with J-BERT's direct external clock mode (Figure 3). The J-BERT pattern generator includes built-in and calibrated sources for random jitter (RJ), sinusoidal jitter (SJ), inter-symbol interference (ISI) injection and automated jitter-tolerance testing. To make unlimited use of J-BERTs internal SJ and SSC jitter sources the external clock signal should be > 6.75 GHz. J-BERT provides clock dividers that achieve the desired UHS-II data rates at its generator outputs.

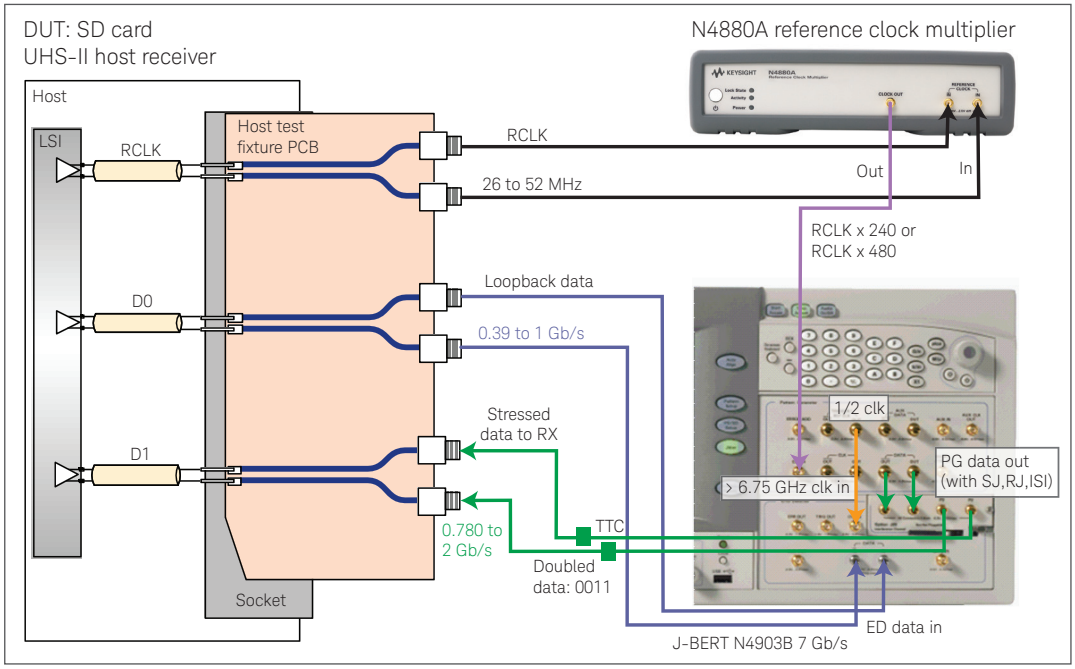

Figure 3. In this configuration, the combination of the N4880A and the J-BERT enables testing of SD UHS-II host receivers. The example shows a recommended setup for bit rates below 1 Gb/s based on UHS-II compliance test specification rev 0.8.

The "double data" mode is suggested when testing bit rates below 780 Mb/s. The J-BERT error detector can run with its built-in clock data recovery (CDR) function at rates above 1 Gb/s. At rates below 1 Gb/s, an external CDR such as N4877A can be used to clock the error detector.

J-BERT can also be used for the testing of receivers in UHS-II devices. In these cases it can generate data and reference clock signals without the N4880A.

Application Example: MIPI M-PHY

MIPI M-PHY receiver test means to overcome several test challenges: this includes testing of one or multiple lanes, support of multiple bit rates (so-called Gear 1, 2, 3 and 4), creating pattern sequences to switch between the device states or switch into loopback mode, jitter injection, emulating compliant channel conditions and handling different ways of error counting.

For MIPI M-PHY receiver test on multiple lanes often a ParBERT 81250A setup is recommended. To test HS Gear 4 devices, the N4880A can be used as shown in Figure 4. A low frequency clock signal with multi-UI in-band jitter (SJ < f_{L_RX}) is generated by a vector signal generator. This can be multiplied by N4880A to be used as jittered high-speed external clock for the ParBERT 13G clock module. This allows locking of ParBERT's generator and analyzer channels on this external clock signal. The N4880A can multiply from all MIPI M-PHY reference clock rates of 19.2, 26, 38.4 and 52 MHz to all high-speed bit rates. However, to achieve lower than HS Gear 4 bit rates the shown vector signal generator can send a high-speed clock itself.

Out-of-band jitter (SJ > f_{L_RX}) and RJ can be generated in addition to the in-band jitter by using ParBERT's delay control inputs modulated by an arbitrary function noise generator such as Keysight 81160A. A clean reference clock signal for the MIPI device can be generated by ParBERT using a second clock group.

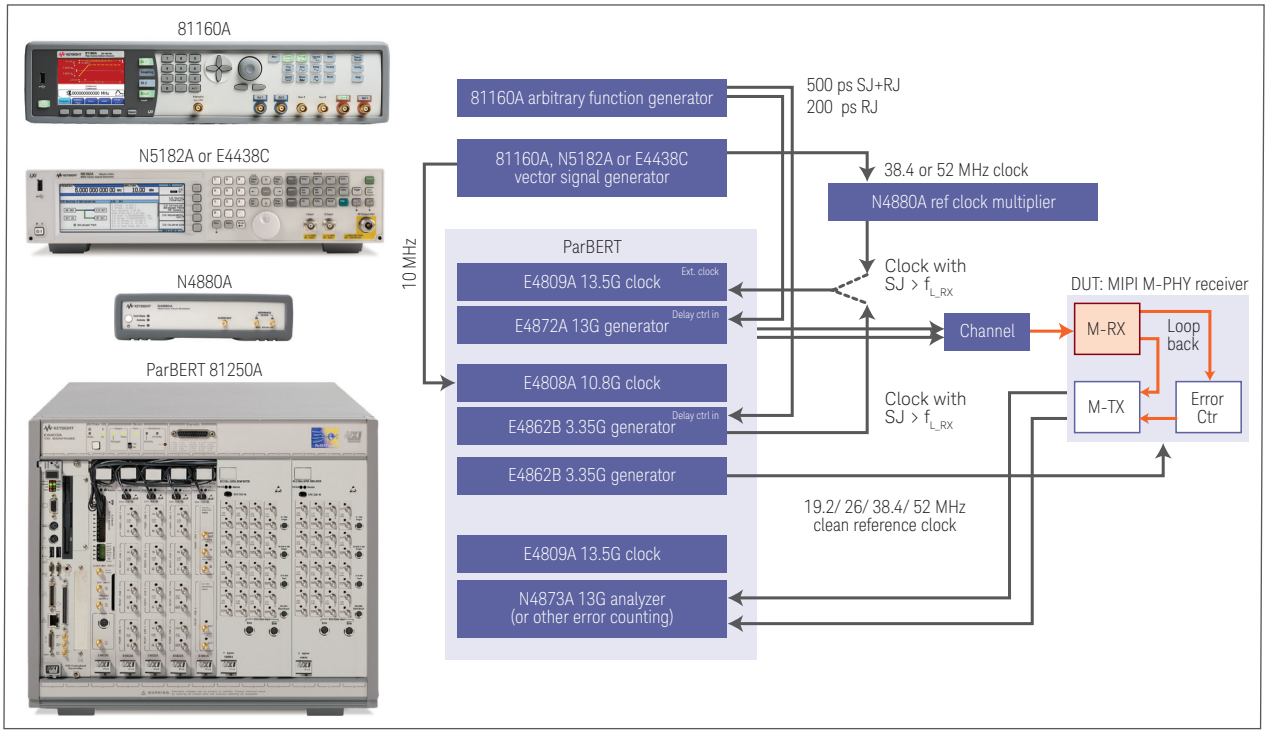

Figure 4. This shows a MIPI M-PHY receiver test setup with the N4880A, ParBERT 81250A and two stress generators. The example shows a HS Gear 4 setup for testing one receiver lane for M-PHY data rates of 9.984, 11.648, or 11.6736 Gb/s.

Specifications for N4880A

Figure 5. Front-panel view of Keysight N4880A reference clock multiplier

Table 1. Specifications for N4880A

Reference clock input	50 Ω differential, DC coupled; unused input must be terminated with 50 Ω
Clock input frequency range	PCIe: 100 MHz MIPI M-PHY: 19.2, 26, 38.4 or 52 MHz UHS-II: 26 to 52 MHz
Clock input voltage range	100 mVpp to 2 Vpp differential
Clock input transition times	< 7.7 ns (20%/80%)
Loop bandwidth	PCIe: typ. 5 MHz MIPI M-PHY: typ. 2 MHz UHS-II: typ. 2 MHz (also see Table 2)
Clock input duty cycle	45 to 55%
Max. input voltage level	–3.0 V to +3.0 V
SSC	Reference clock input tolerates up to 3% SSC down-spread modulated with 33 kHz for 26 MHz reference clocks
Clock output	50 Ω single-ended, DC coupled. Can drive J-BERT or ParBERT 7G/13G pattern generator
Clock multiplier factors	See Table 2
Clock output range	6.240 to 13.500 GHz[1]
Clock output voltage	Typical 300 to 600 mVpp, not adjustable
Output jitter	Typical 1.9 ps rms RJ additional intrinsic jitter at reference clock 2 ns (20%/80%) transition time, 100 mVpp Typical 2.1 ps rms RJ additional intrinsic jitter at reference clock 7.7 ns (20%/80%) transition time, 100 mVpp.
Output transition time	Typical < 25 ps (20%/80%), not adjustable
Output duty cycle	Typical 50% ±5%, not adjustable
Connectors front panel	SMA 3.5 mm, female
Connectors rear panel	USB; IEC power connector

1. For instruments with S/N < MY52400150: 6.24 GHz to 12.48 GHz

Specifications for N4880A (continued)

Table 2. Multiplier factors for N4880A

Digital bus standard	Reference clock input	Target bit rate	N4880A output clock	PLL loop bandwidth	N4880A multiplier	Recommended CLK IN divider in pattern generator to achieve target bit rate[1]
PCI Express 3	100 MHz	8 GHz	8 GHz	5 MHz	80	1
PCI Express 2	100 MHz	5 GHz	10 GHz	5 MHz	100	2
PCI Express 1	100 MHz	2.5 GHz	10 GHz	5 MHz	100	4
MIPI M-PHY	19.2 MHz	1.248 GHz	9.984 GHz	2 MHz	520	8
MIPI M-PHY	19.2 MHz	1.4592 GHz	11.6736 GHz	2 MHz	608	8
MIPI M-PHY	19.2 MHz	2.496 GHz	9.984 GHz	2 MHz	520	4
MIPI M-PHY	19.2 MHz	2.9184 GHz	11.6736 GHz	2 MHz	608	4
MIPI M-PHY	19.2 MHz	4.992 GHz	9.984 GHz	2 MHz	520	2
MIPI M-PHY	19.2 MHz	5.8368 GHz	11.6736 GHz	2 MHz	608	2
MIPI M-PHY	26 MHz	1.248 GHz	9.984 GHz	2 MHz	384	8
MIPI M-PHY	26 MHz	1.456 GHz	11.648 GHz	2 MHz	448	8
MIPI M-PHY	26 MHz	2.496 GHz	9.984 GHz	2 MHz	384	4
MIPI M-PHY	26 MHz	2.912 GHz	11.648 GHz	2 MHz	448	4
MIPI M-PHY	26 MHz	4.992 GHz	9.984 GHz	2 MHz	384	2
MIPI M-PHY	26 MHz	5.824GHz	11.648 GHz	2 MHz	448	2
MIPI M-PHY	38.4 MHz	1.248 GHz	9.984 GHz	2 MHz	260	8
MIPI M-PHY	38.4 MHz	1.4592 GHz	11.6736 GHz	2 MHz	304	8
MIPI M-PHY	38.4 MHz	2.496 GHz	9.984 GHz	2 MHz	260	4
MIPI M-PHY	38.4 MHz	2.9184 GHz	11.6736 GHz	2 MHz	304	4
MIPI M-PHY	38.4 MHz	4.992 GHz	9.984 GHz	2 MHz	260	2
MIPI M-PHY	38.4 MHz	5.8368 GHz	11.6736 GHz	2 MHz	304	2
MIPI M-PHY	52 MHz	1.248 GHz	9.984 GHz	2 MHz	192	8
MIPI M-PHY	52 MHz	1.456 GHz	11.648 GHz	2 MHz	24	8
MIPI M-PHY	52 MHz	2.496 GHz	9.984 GHz	2 MHz	192	4
MIPI M-PHY	52 MHz	2.912 GHz	11.648 GHz	2 MHz	192	4
MIPI M-PHY	52 MHz	5.824 GHz	11.648 GHz	2 MHz	224	2
MIPI M-PHY	52 MHz	5.824 GHz	11.648 GHz	2 MHz	224	2

Specifications for N4880A (continued)

Table 2. Multiplier factors for N4880A

Digital bus standard	Reference clock input	Target bit rate	N4880A output clock	PLL loop bandwidth	N4880A multiplier	Recommended CLK IN divider in pattern generator to achieve target bit rate[1]
For S/N >MY52400150 with software rev 1.10 or higher:						
SD UHS-II	26 to 28.125 MHz	0.390 to 0.421875 GHz	12.48 to 13.5 GHz	2 MHz	480	16 + data doubling
SD UHS-II	28.125 to 52 MHz	0.421875 to 0.780 GHz	6.75 to 12.48 GHz	2 MHz	240	8 + data doubling [2]
SD UHS-II	26 to 28.125 MHz	0.78 to 0.84375 GHz	12.48 to 13.5 GHz	2 MHz	480	8 + data doubling [2]
SD UHS-II	28.125 to 52 MHz	0.84375 to 1.560 GHz	6.75 to 12.48 GHz	2 MHz	240	4 + data doubling [2]
For S/N < MY52400150:						
SD UHS-II [3]	26 to 52 MHz	0.390 to 0.780 GHz	6.24 to 12.48 GHz	2 MHz	240	16
SD UHS-II [3]	26 to 52 MHz	0.780 to 1.56 GHz	6.24 to 12.48 GHz	2 MHz	240	8

1. 7G versions of J-BERT N4903B and ParBERT 81250 can be used, even if N4880A output clock rate is higher than 7 GHz.
2. Data doubling means that the pattern bits must be doubled (e.g. 01 becomes 0011). Alternatively to data doubling, the CLK IN divider factor in the pattern generator could be doubled to achieve the target bit rate.
3. Instruments with S/N below MY52400150: for reference clocks that operate between 26 MHz and < 28.125 MHz and when performing SJ injection, an N4916B-001clock doubler must be applied between the reference clock multiplier output and the J-BERT external clock input. In addition, the pattern generator bits must also be doubled (e.g., 01 becomes 0011) to compensate for the clock doubling.

Figure 6. Rear-panel view of Keysight N4880A reference clock multiplier

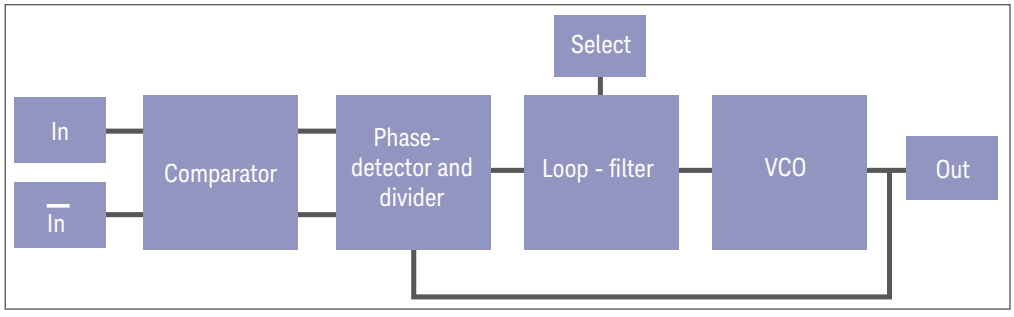

Figure 7. Block diagram of N4880A multiplying PLL

Specifications for N4880A (continued)

Table 3. General characteristics for N4880A

Power consumption	100–240 V, ~50/60 Hz, 80 VA max
Operating temperature	5 to 40°C (–23 to 104°F)
Storage temperature	–40 to 70° C
Operating humidity	95% relative humidity non-condensing
Storage humidity	50% relative humidity
Physical dimensions (WxHxD)	Bench top with bumper and connectors: 228 x 59 x 240 mm (9.0 x 2.3 x 9.74 in)
Rack mount without bumper	1/2 x 19" width, 1U height
Weight net	1.9 kg (4.2 lb)
Weight shipping	~4.5 kg (10 lb)
Regulatory standards	
Safety	IEC61010-1:2001, EN61010-1:2001, CAN/CSA-C22 No. 61010-04, UL 61010-1:2004
EMC	IEC61326-1:1997+A1:1998, EN61326-1:1997+A1:1998
Quality management	ISO 9004, ISO 14000
Remote control interface	
Connectivity	USB2.0, rear panel
Programming language	Command line programming interface, SCPI extension on J-BERT N4903B SW 7.2 or higher
Standalone user interface	Graphical, color user interface
System requirements	Operating system: Microsoft Windows XP, SP3 (32 bit), or Vista SP2 (32 and 64 bit), or Windows 7 SP1 (32 and 64 bit) Microsoft .NET 2.0 SP2 To use the J-BERT SCPI remote extension, N4903B software 7.2 or higher is needed

Specification Assumptions

The specifications in this document describe the instruments warranted performance.

Non-warranted values are described as typical.

All specifications are valid in a range from 5 to 40°C ambient temperature and after a warm-up phase of 30 minutes.

If not otherwise stated, all inputs and outputs need to be terminated with 50 Ω to GND. All specifications are valid using the recommended cable SMA cable set.

Ordering Information

Model Number	Description
N4880A	Reference clock multiplier; included accessories: One 50 Ω termination, 3.5 mm; USB cable; CD-ROM with software and user documentation; functional test report; ROHS addendum
15442A	Four SMA-to-SMA cables, unmatched, for clock in and out
15443A	Matched SMA-to-SMA cable pair
N4235-61602	SMP-to-SMA cable pair for PCIe CEM testing
E5810A-100	Rack-mount kit
R1280	Calibration service
R1380-N49xx	Productivity assistance

Related Literature

Title	Publication number
J-BERT N4903B High-Performance Serial BERT – Data Sheet	5990-3217EN
PCI Express 3.0 Calibration Channels – Data Sheet	5990-7659EN
N4916B 4-Tap De-Emphasis Signal Converter – Data Sheet	5990-4630EN
Infiniium 90000 X-Series Oscilloscopes 16-32 GHz True Analog Bandwidth – Data Sheet	5990-5271EN
Infiniium DSO90000 Series High-Performance Oscilloscopes – Data Sheet	5989-7819EN
N5990A Test Automation Software Platform – Data Sheet	5989-5483EN
How to Pass Receiver Test According to PCI Express 3.0 CEM Specification – Application Note	5990-9208EN
Accurate Calibration of PCIe 3.0 Receiver Stress Signals (Base Spec) – Application Note	5990-6599EN
PCIe 2.0 Receiver Testing with J-BERT N4903B – Application Note	5990-3233EN

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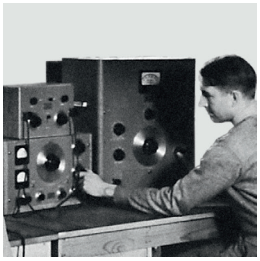
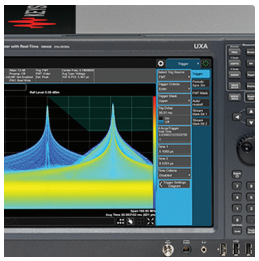


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