Keysight Technologies

PAM-4 Design Challenges and the Implications on Test

Application Note

KEYSIGHT TECHNOLOGIES

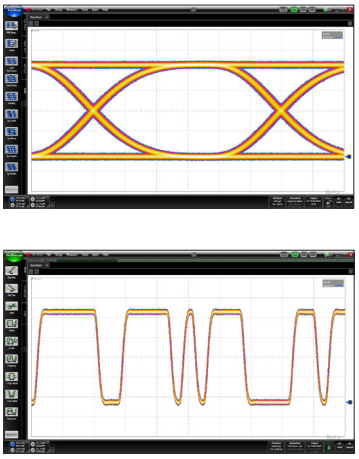
Ever-increasing demands for a connected world with instant data access continues to drive Ethernet transmission innovation. Development of 100G Ethernet data transmission is currently in production and will continue to evolve. Achieving 400G Ethernet represents a significant and disruptive technological step. Technological advances towards achieving greater Ethernet speed presents two design possibilities, NRZ and PAM-4, and each comes with a unique set of challenges.

NRZ (Non-Return-to-Zero) uses a currently available technology and will continue a linear evolution from 100G (25/28G, 4 lanes) to 400G (56G, 8 lanes). From a time domain perspective, NRZ consists of 1's and 0's and can be referred to as PAM-2 (pulse amplitude modulation, 2-level) for the two amplitude levels that contain 1 bit of information in every symbol (Figure 1). The NRZ eye diagram (Figure 1), providing timing and voltage used to measure link performance, contains a single eye.

Since NRZ has gradually evolved over the last 50 years with improved speed from 10G to 100G, many new concepts have had to be researched and addressed. These same concepts will continue to need advanced technology to achieve the higher 400 Gb/s data rate.

The familiar challenging concepts for NRZ include totally closed eyes, shorter unit intervals (UI), tighter jitter requirements, and the mandatory use for forward error correction (FEC). The closed eye issue causes triggering difficulties as with 100G, but with more channel loss at 400G and requires enhanced receiver equalization such as continuous-time-linear equalization (CTLE) and decision feedback equalization (DFE) to correct. Standards are requiring increased receiver sensitivity (down to 50 mV). Jitter budgets are even tighter for 400G at 17ps UI and may be below intrinsic jitter of test equipment. FEC, a technique used for controlling errors in data transmission over unreliable or noisy communication channels, becomes a greater challenge with increased noise at the faster data rate. For the most part, channel loss and reflections (noise) are expected to be the biggest NRZ technological challenge as it continues its linear growth path.

NRZ (PAM-2)



- 2 amplitude levels
- 1 bit of information in every sysmbol

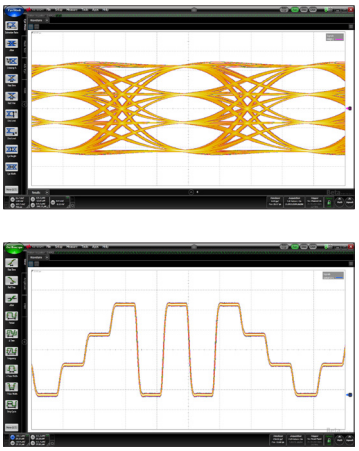
Figure 1. NRZ eye diagram (top), NRZ (PAM-2) amplitude levels (bottom)

PAM-4 Design and measurement challenges

PAM-4 (Pulse Amplitude Modulation, 4-level) from a time domain perspective has four digital amplitude levels (-3, -1, 1, and 3), as shown in Figure 2. PAM-4 has an advantage over NRZ in that for each level ("symbol") there are 2 bits of information providing twice as much throughput for the same Baud rate (28 GBaud PAM-4 = 56 Gb/s). From a frequency domain perspective, PAM-4 requires half the bandwidth of that of NRZ. In the PAM-4 eye view (Figure 2), you can see 3 vertical eyes created by the 4 levels. Unlike NRZ, where the decision level is fixed to 0 V for a differential signal, the three slicer levels used by a PAM-4 receiver can be adaptive, or time varying.

The use of multi-level signaling for PAM-4 has entirely changed what has been expected in Ethernet test in the past. Newly developed technology is required to accomplish implementation of PAM-4 components and serial links with changes to system test as more complex transmit and receive circuit designs are required to address PAM-4 challenges. PAM-4 technical challenges include a shift from saturating output stages to linear IO behavior in order to achieve multiple levels. New chip designs face the challenge of managing the size of the integrated circuits (ICs) supporting PAM-4 which have increased nearly 30%. The larger IC size is due to additional linear drivers and detectors and has resulted in up to 35% increase in power requirements as well. For Ethernet chips with large IO counts, the problems are even greater.

PAM-4



- 4 amplitude levels
- 2 bits of information in every sysmbol (2x throughput for the same Baud rate)
- lower SNR, more susceptible to noise

Figure 2. PAM-4 eye diagram (top), PAM-4 amplitude levels (bottom)

PAM-4 Design and measurement challenges *continued*

Data transmission advancement using PAM-4 includes many new design and test challenges. Research will continue to determine how to address many PAM-4 challenges such as:

- Clock Recovery. Finite rise time acting on different transition amplitudes creates inherent inter symbol interference (ISI) and makes clock recovery much more difficult. Transition time of the PAM-4 data signal can create significant horizontal eye closure due to switching jitter, which is dependent on the rise and fall time of the signal. Transition qualified phase detectors are needed to look at analog levels for clock recovery. Whether direct detection (comparators), which require a lot of power, or digitizing ADCs, which are expensive, are used is still to be determined.
- Decision Feedback Equalization (DFE). DFE is used to calculate a correction value that is added to the logical decision threshold and results in the threshold shifting up or down so new logical decisions can be made on the waveform based upon the new equalized threshold level. The technology required to manage DFE and the possible addition or use of other equalizers for PAM-4 multi-levels is still to be determined.
- Loss of Signal to Noise Ratio (SNR). The PAM-4 signal has 1/3 the amplitude of that of a similar NRZ signal (SNR loss of ~9.5 dB) due to level spacing and is more susceptible to noise. However, it is possible that the lower PAM-4 insertion loss compensates for the 9.5dB loss in SNR due to reduced signal amplitude in PAM-4 signaling.

PAM-4 Simulation and test

Typical PAM-4 communications system configurations for transmitter (TX), channel, and receiver (RX) can be chip-to-chip, chip-to-module (electrical or optical) or electrical backplane. Development of these high performance components, modules and networks requires sophisticated test and measurement techniques for interface interoperability and test validation. For NRZ 400G design, there are decades of experience to base new development on. Unlike NRZ, few teams have done much PAM-4 simulation. This makes augmenting PAM-4 system simulation very valuable. New considerations for tests and end-to-end link simulation will be essential to verify PAM-4 compliance and ensure interoperability. During simulation and test at the higher data rates it is also important to keep in mind that test instruments must be more capable than what they are intended to measure. For example, 10 Gb/s is 100 ps and increasing speed to 25 Gb/s relates to 40 ps, so the higher link jitter is at or beyond the capability of some instruments.

The challenge of device design validation and test increase as the data rates increase not only due to noise susceptibility, but also test probe or fixture interference. As cables and test fixtures are inserted between the device under test and test equipment, one may not expect to create a notable influence on the signal. However, at higher data rate transmissions, noise and interference become significant factors. Device test interference can occur from simple insertion of measurement instruments. For example, random noise can be induced from the device transmitter and then it root-sum-square adds to the intrinsic random noise from a measuring oscilloscope. In this case, it is important to know what the oscilloscope noise is for the bandwidth and gain being measured so it can be removed or de-embedded from the signal. Signal loss even in test cables at higher speeds is significant and may require de-embedding.

PAM-4 Simulation and test *continued*

Typically, engineers design test fixtures with a controlled impedance environment so the fixture effects can be minimized, but it is impossible to completely eliminate skin effect series trace loss, dielectric shunt loss and inductive or capacitive impedance discontinuities of the fixture channel. Test fixture deficiencies cause signal loss and reflection with increased effects at higher frequencies. A few different approaches used to remove the test fixture effects from the measurement include direct measurement (pre-measurement process) and de-embedding (post-measurement processing). Direct measurement uses specialized calibration standards that are inserted into the test fixture and measured. De-embedding uses models (like Touchstone or citifile) of the test fixture and mathematically removes the fixture characteristics from the overall measurement. De-embedding methods require that an accurate characterization model of the fixture be obtained first. Examples of de-embedding methods include “simulation-based” and “calibration-based”. The simulation based method simulates the waveform before the fixture is fabricated. The calibration-based method is used to eliminate fixture effect after the fixture is available for use during the measurement process.

Simulation modeling is very important, especially for PAM-4 as new designs are developed and expertise is built. Simulations help to provide evaluation and performance prediction of a specific portion of a link or a complete end-to-end link design. Complex behaviors of NRZ transmitter and receiver signals have been modeled using the Algorithmic Modeling Interface (AMI) standard. AMI is a behavioral model first defined in the Input/Output Buffer Information (IBIS) 5.0 specification and provides both passive channel characteristics and SerDes functionalities. The current AMI standard supports NRZ signaling assuming the TX signal has two levels and the receiver slicer reference is at 0V. The AMI Simulation flow for NRZ can be seen in Figure 3 with a 2-level input waveform and output waveform with clock data recovery (CDR) times.

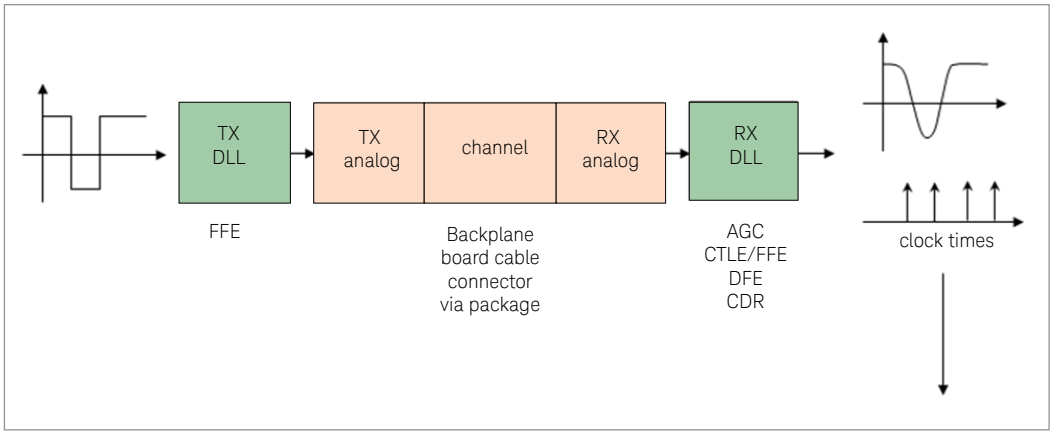


Figure 3. NRZ Simulation Model

PAM-4 Simulation and test *continued*

AMI simulation flow development for PAM-4 modeling will be more challenging with a multi-level input signal for transmitter coding schemes (Figure 4). In addition to the output waveform and CDR clock times, for PAM-4 simulation, transient behavior of the slicer reference levels (DT, DM and DB in Figure 5) and the sampling time skews between slices are captured by AMI models and used by the simulator to calculate the eye diagram and symbol error rate (SER).

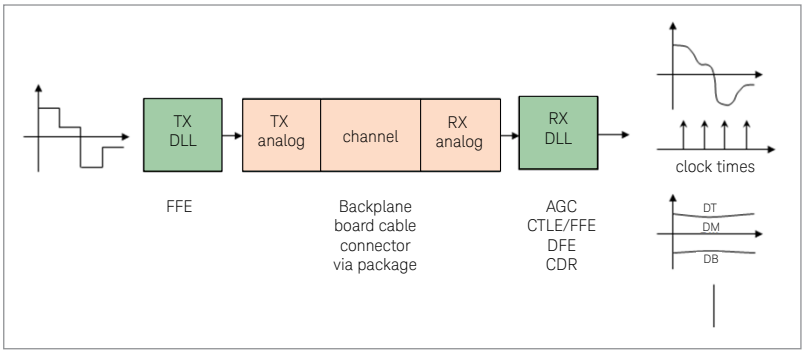


Figure 4. PAM-4 Simulation Model

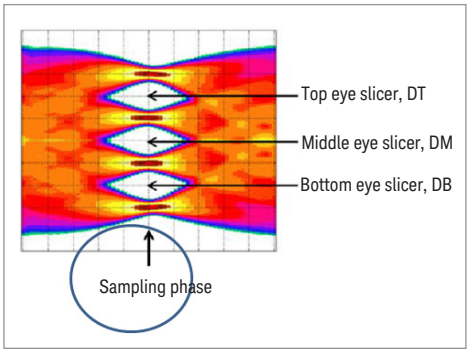


Figure 5. PAM-4 Transient Slicer Levels

The ability to test and rectify effects of interference at the higher data transmission rate and to research new circuit, module and network technology required for PAM-4 designs depends on successful PAM-4 simulation. Electronic Design Automation (EDA) tools such as the Keysight Advanced Design System (ADS) bundle for signal integrity enables designers to address the simulation-measurement correlation and workflow for Ethernet PAM-4 and NRZ. ADS channel simulation allows 1E6 bits in minutes, not hours, while enabling industry leading simulation accuracy with convolution.

Measurement solutions

Measurement and simulation challenges for PAM-4 are similar and the key challenges facing engineers today are clock recovery (CR), eye skew and noise.

Transmitter (TX) or output testing, verifies that factors such as eye parameters and jitter measurements meet or exceed standard requirements and most often uses an oscilloscope. Receiver (RX) or input testing verifies that the correct bits are detected with impairments from a worst case channel traditionally using a Bit Error Ratio Tester (BERT) as the principle measurement tool. System testing verifies the TX/RX device works in a system under all conditions and can use many different measurement tools such as oscilloscopes, BERTs, protocol analyzers, etc. With PAM-4 there are new complexities that increase measurement challenges. Test and measurement in these early stages of PAM-4 links is helping to build an understanding of the causes and mechanisms of artifacts that impair link error performance. Impaired links can be related to implementation of clock recovery, and closed eye challenges such as skew, compression and nonlinearity. As the PAM-4 technology continues to advance and knowledge of PAM-4 challenges and solutions grows, new measurements will emerge to characterize transmitter outputs and new stress impairments will be developed to test and characterize receiver inputs.

Measurement solutions *continued*

For the higher 56 Gb/s data rate, equalization is mandatory. Due to the increased signal rate, the channel the signal travels through distorts the signal at the receiver. The result can be seen using an oscilloscope and show a partially or completely closed eye diagram (Figure 6) that will prevent the receiver's ability to extract the clock and/or data. Equalization needs to be applied to re-open the eye diagram correcting for the intersymbol interference (ISI) and recover the clock or data. Equalization methods used include feed forward equalization (FFE) for the transmitter and continuous-time-linear equalizer (CTLE), decision feedback equalizer (DFE) and CDR for the receiver. Clock recovery tracks low-frequency jitter and is utilized by either a real-time oscilloscope or a sampling oscilloscope when characterizing a transmitter. Today's oscilloscopes include software that can be used to model equalization such as CTLE, DFE and FFE. An example is the Keysight N5461A Infiniium Serial Data Equalization Software which allows the user to choose which equalizer, or combination, they want to implement.

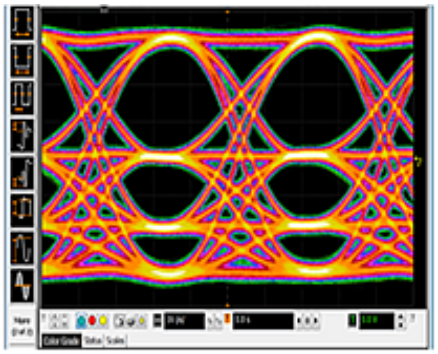


Figure 6. Non-linearity - amplitude compression in lower eyes

PAM-4 receivers can be impaired by time skew from eye to eye resulting from the optical output of a vertical cavity surface emitting laser (VCSEL) in a fiber optic transceiver driven by a PAM-4 signal. VCSELs turn on faster when driven with a higher voltage, causing the lower transition eye to lag the upper two eyes (Figure 7). The alignment of the upper, middle and lower eyes is defined in PAM-4 standards. At high baud rates, the skew can be great enough to require different detection sampling times for each transition eye. More complex PAM-4 receiver designs will be needed to address the sampling delay per eye.

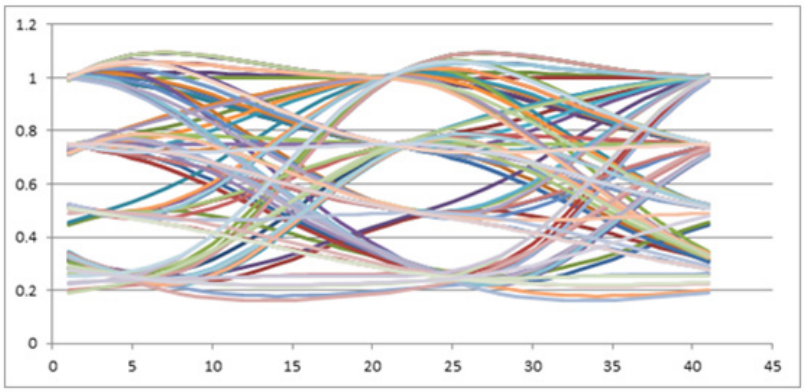


Figure 7. VCSELs turn on faster when driven with a higher voltage, resulting in eye skew

Higher data rate transmissions cause a change in signal characteristics and additional error correction techniques are needed to maintain an open eye. Non-linearity or amplitude compression can alter the eye height of different transition eyes causing a linearity error due to a lower signal to noise ratio of the lower transitions.

Output transmitter (TX) characterization

Transmitter testing verifies that the output parameters meet or exceed the standard requirements including eye parameters and jitter measurements. The types of measurements required to characterize the transmitter output will continue to grow and improve as PAM-4 development progresses.

According to Clause 94 in IEEE 802.3-2014, PAM-4 transmitters must be capable of generating simple test patterns such as JP03A and JP03B. The pattern defined as JP03B is used to measure random jitter (RJ), uncorrelated deterministic jitter or periodic jitter (PJ), and even-odd (F/2) jitter.

- JP03A Test Pattern (repeating {0,3} sequence)
- JP03B Test Pattern ({0,3} is repeated 15 times then, {3,0} is repeated 16 times) Also defined as a 62 bit clock pattern with phase reversal.

PAM-4 linearity is a very important parameter that can be tested with the standard Transmitter Linearity Test Pattern (Figure 8). Each of the four PAM-4 levels can be measured for mean voltage, power if optical, or noise. The pattern is also used to analyze the transmitter linearity by measuring minimum signal level (Smin), effective symbol levels (ES1 and ES2), and level separation mismatch ratio (RLM)

- Transmitter Linearity Test Pattern (repeating 160 symbol patterns with a sequence of 10 symbol values, each 16 UI in duration)
- 10 consecutive symbols mitigates the impact of ISI on “Level” measurements (VA, VB, VC, VD)

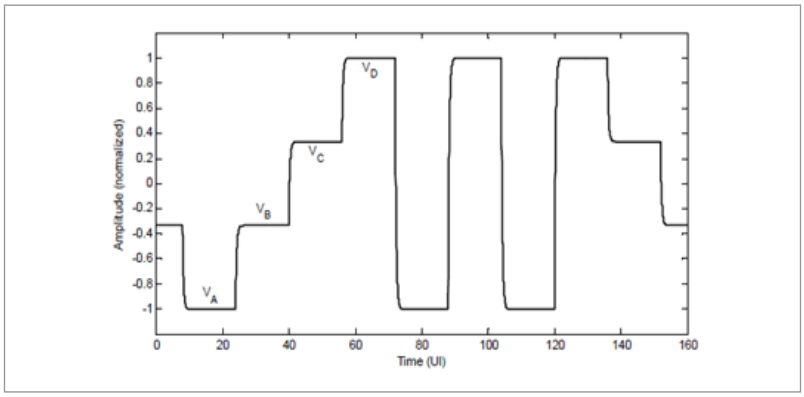


Figure 8. Transmitter linearity test pattern

Eye height, eye width, and eye skew are key parameters of transmitted PAM-4 signals and can be tested with the standard Quaternary PRBS13 Test Pattern.

- Quaternary PRBS13 Test Pattern (QPRBS13) which is a repeating 15548 symbol (338 training frame words) sequence.

Output transmitter (TX) characterization *continued*

Level, the mean "thickness", and skew are also measured (Figure 9). There are two different types of PAM-4 receivers being considered for development; a slicer level based receiver where eye height/width are important, or an ADC based receiver where level variation in constellation form is most important. The Quaternary test pattern can be used to verify transmitter outputs for either receiver design.

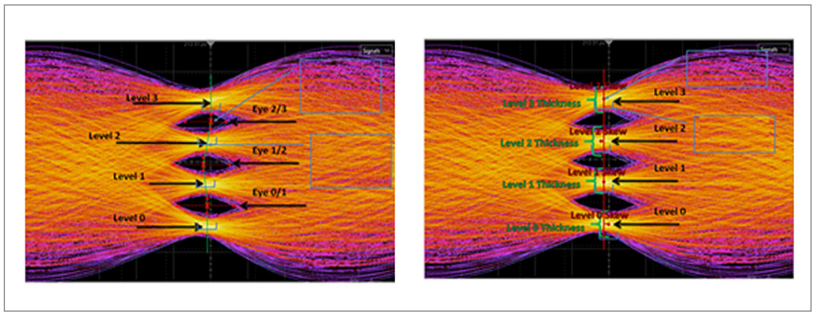


Figure 9. Eye centric measurements (left), level centric measurements (right)

Keysight provides instrument solutions for the test and measurement of transmitter signals. Transmitter (TX) characterization can be performed by real-time or equivalent-time (sampling) oscilloscopes. As mentioned earlier, PAM-4 signals have a lower SNR than NRZ, so added noise as a result of the oscilloscope becomes an important consideration. Due to their hardware architecture, sampling oscilloscopes have an inherent noise floor that is very low compared to real-time oscilloscopes having comparable bandwidth, and as a result, will often yield the most accurate characterization of a PAM-4 signal. The Keysight 86100D with 86108B (Figure 10) is a sampling oscilloscope that provides high signal fidelity due to its wide bandwidth (>50 GHz), ultra-low timebase jitter (RJ<45 fs rms), low noise floor, (<800 µV) together with an integrated clock recovery that operates on NRZ and PAM-4 signals to 32 GBaud. With 86100D-9FP PAM-N Analysis software, the 86100D DCA-X provides PAM-4 measurements such as level mean/thickness/skew, eye mean/height/width/skew, and linearity. For optical PAM-4 systems, the Keysight 86100D DCA-X with 86105D-281 provides up to 2 optical channels per module. The DCA can also be configured to analyze up to 16 electrical PAM-4 signals simultaneously using the N1045A 60 GHz Electrical or N1055A 50 GHz TDR/TDT modules.

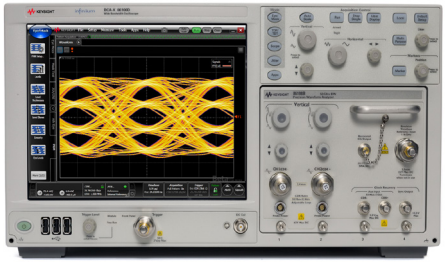


Figure 10. 86100D Infiniium DCA-X Wide-Bandwidth Oscilloscope

Transmitter characterization can also be measured using a real-time oscilloscope such as the Keysight DSO/DSAZ634A (Figure 11) which is best for troubleshooting and single shot events. The real-time oscilloscopes provide the fastest sample rate (160 G Sa/s), large record length (deep single-shot memory) and do not require repetitive signals to generate pattern waveforms. New PAM-4 algorithms are required for real-time oscilloscopes which use software for clock recovery. Software for the real-time scopes can capture PAM-4 measurements such as eye width/height @ BER and equalization (FFE/CTLE). N8827A/B PAM-4 analysis software for Infiniium real-time oscilloscopes accurately and quickly characterizes PAM-4 electrical signals described in IEEE 802.3bj Clause 94. The PAM-4 analysis software also addresses future measurement needs as outlined in developing standards such as OIF-CEI-56G and IEEE 400G. Data pattern generation can be achieved by using a second DUT, BERT or arbitrary waveform generator.

Figure 11. DSAZ634A Infiniium 63 GHz Real-Time Oscilloscope

Input receive (Rx) characterization

Input testing verifies that the receiver is able to detect correct bits along with impairments from a worst case channel. PAM-4 receivers are more susceptible to linearity and skew problems. The inherent ISI in the PAM-4 eye requires receivers to be much less sensitive to pattern dependent jitter. As PAM-4 receiver technology progresses, new types of stress impairments will need to be developed for testing the receiver inputs.

Figure 12. M8020 J-BERT High-Performance BERT

Similar to the NRZ receiver, the traditional tool for PAM-4 receiver characterization and input testing will continue to be the Bit Error Ratio Tester (BERT) (Figure 12), which provides pattern generation and error detection. Some of the emerging 400G standards require PAM-4 devices to have integrated bit error measurement capability. These circuits provide simple link testing, but have no calibrated impairments. Thus a key focus for BERTs used for PAM-4 input testing will be on the pattern generator side. Error analyzers will continue to be offered for simpler devices which lack built in test capability.

Methods of PAM-4 pattern generation

There are two approaches for generating PAM-4 patterns for receiver testing. The most common is based on traditional BERT NRZ pattern generators (Figure 13). Two channels of pattern aligned data streams, representing the most and least significant bits, are combined together to create the PAM-4 signal. The output representing the least significant bit (LSB) is attenuated 6 dB relative to the other output. A delay equal to the attenuation path is added in the output representing the most significant bit (MSB), and the two signals are summed together using an RF power divider. In practice, two attenuators are often used, a 10 dB and a 3 dB. The attenuation in both paths reduces the effect of reflections from mismatch in the transmission lines, which cause problems in PAM-4 systems. 10 dB is used in the LSB output, as 9 dB attenuators are not commonly available. The 1 dB error is corrected with the amplitude controls in the pattern generator outputs.

As with most choices, there are trade-offs between the two pattern generation methods. The combining outputs of NRZ BERTs described above allows long patterns, limited only by the length of user memory in the BERT. It also has potentially faster rise and fall times assuming proper selection of the attenuators and RF power divider. Faster rise times are important for using the generator as a golden transmitter emulator, but not for receiver input testing, as channels are generally used to slow the edges down even further. This approach can be expensive, as two high performance pattern generator outputs are required to generate a single channel of PAM-4 pattern.

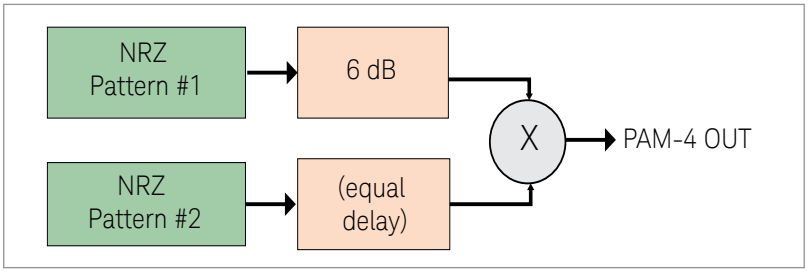


Figure 13. PAM-4 pattern generation utilizing a BERT

Methods of PAM-4 pattern generation *continued*

The greatest limitation of the combining two NRZ pattern approach is the limited types of impairment or "stress" generation. NRZ BERTs can create a variety of timing related stress types such as sinusoidal, random, bounded uncorrelated and F/2 jitters, but very little amplitude related stress types. A traditional NRZ BERT may have interference (amplitude noise) injection, but this will be applied evenly to all parts of the PAM-4 signal. As discussed earlier, PAM-4 receivers are sensitive to linearity and individual eye skews in the PAM-4 waveforms. These types of stress can not be adequately generated using NRZ BERTs.

An alternative to BERT, is an arbitrary waveform generator (AWG) and the recommended M8195A 65 GS/s AWG (Figure 14) is a very flexible product providing up to 32 Gbaud for a broad variety of modulation schemes. The recent M8195A breakthrough in speed allows it to be considered as a solution for generating communication signals. The AWG offers the benefit of not being limited to PAM-4 signals and can generate any amplitude modulated signal such as PAM-8, coherent, OFDM, and QAM-N. The M8195A's fractional re-sampling allows generation of fine resolution jitter and other impairment distortions. Stress types including jitter, interference, skew, linearity and more can be easily generated. As standards evolve, new stress types can be easily added since they are created in the math simulator making the AWG future ready. A smaller form factor and lower cost make the AWG even more attractive. Relative to the BERT, the M8195A AWG pattern lengths are limited but the defined PAM-4 test patterns can be easily generated. The AWG rise times are fast enough to emulate channels for receiver testing since additional slowing from the channel is needed. Additionally, there is a new M8195A software GUI that "drives like a BERT" making pattern generation easy.

Figure 14. M8195A 65 GSa/s Arbitrary Waveform Generator

A new, powerful software tool FlexDCA (Figure 15) provides a way to quickly create and generate new stress types when combined with the 86100D DCA-X and M8195A AWG. FlexDCA runs inside the DCA sampling oscilloscope or standalone, and you can view the waveform results as math processing is quickly added. Waveform source can be a saved measurement or simulated. The key advantage of the FlexDCA software tool is that it can be used to amplify suspected anomalies found using the DCA oscilloscope creating new stress PAM-4 patterns in minutes.

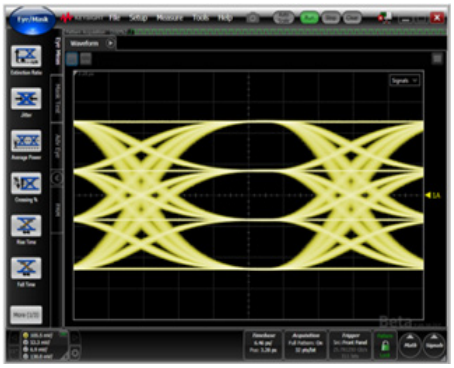


Figure 15. FlexDCA software enables fast stress pattern generation

Additionally, as mentioned earlier, EDA tools such as the Keysight ADS bundle for signal integrity enables designers to address the simulation-measurement correlation and workflow for Ethernet PAM-4 and NRZ. ADS simulation output can be sent directly to the FlexDCA. Common algorithms between simulation and hardware results reduce a fundamental measurement uncertainty, increasing the systematic value of simulation data.

Managing optical signals

Long distance Ethernet links are optical and require conversion for testing with electrical test equipment. Electrical-to-optical-to-electrical physical layer design simulation is just as critical and available via EDA tools such as SystemVue or ADS. For transmitter testing, sampling oscilloscopes with optical plug-ins or real-time oscilloscopes with instrument grade optical/electrical (O/E) converters (detectors) are available. Electrical interconnections must be carefully managed through calibration for loss and reflections. For receiver testing with BERTs, a second DUT (stable and calibrated) can be used as a laser source. A second DUT can also be used as an O/E to feed the error detector from the back channel. It is important in this case to ensure the optical detector BER is significantly lower than the measurement.

Summary

As Ethernet technology progresses from 100G to 400G, new test technology, measurement capabilities, and ability to accurately simulate PAM-4 designs for TX and RX hardware are mandatory. The change from NRZ to PAM-4 multi-level signaling presents many new design and measurement challenges.

During design simulation, NRZ historical information from prior generations can be applied to the design. As the industry moves to PAM-4, early simulation of the design with EDA tools will become more critical. Common algorithms between simulation and hardware results reduce a fundamental measurement uncertainty, increasing the systematic value of simulation data. PAM-4 transmitter output testing will continue to use sampling and real-time oscilloscopes with built-in measurements that will evolve with the PAM-4 technical needs. PAM-4 input testing can be accomplished with the traditional BERT approach for pattern generation. However, development of new stress types will be required to emulate impairments and new enabling technologies will evolve. Modern high-speed AWGs can provide stressed patterns for PAM-4, and for complex modulation schemes in the future. Keysight engineers are working at the forefront of Ethernet technology and migration to 400G to help you navigate as the technology evolves. Keysight continues to provide powerful solutions for emerging technologies such as PAM-4.

Standards

The progress of PAM-4 development first requires agreed upon standards to ensure compliance and interoperability of PAM-4 technology. There are several organizations investigating PAM-4 that are in various states of progress.

- **Ethernet**
  The Ethernet standard provides electrical and optical links between equipment, backplanes and cables. The IEEE 802.3bj clause 94 (25.78Gb/s as 13.6 GBaud PAM-4 in 1m backplane) has been implemented and is being used in PAM-4 signaling today. The adoption rate of this standard is slow due to minimal advantages and lack of performance improvements for reach and connector interfaces over the previous clause 93-25.78 G NRZ.
- **OIF-CEI (Optical Internetworking Forum - Common Electrical Interface)**
  The CEI standard provides electrical links for chip-to-chip, chip-to-module, backplane and cables. Each standard covers a narrow range of data rates. OIF-CEI 4.0 (56G-VSR, MR, LR) addresses 28G and work is beginning for 56G. The CEI standards are the basis for other standards pertaining to Ethernet, Fiber channel, Infiniband.
- **InfiniBand**
  The Infiniband standard provides electrical and optical links between supercomputing equipment. PAM-4 proposals are being discussed that would support 400 GbE Chip-to-Chip (c2c) and Chip-to-Module (c2m) as well as PAM-4 ability to work on existing CAUI-4 (100G) infrastructures.
- **Fibre Channel**
  Fibre Channel provides optical links between data center equipment. Currently, 32GFC is complete, 128G (4x32) is in progress and 64G Fibre Channel standard is still under discussion.

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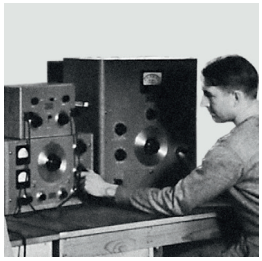

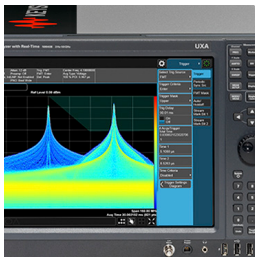

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Published in USA, December 1, 2017
5992-0527EN
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