

# M8040A High-Performance BERT 64 Gbaud

Version 8.0

## Master your next design

New features:

- PCIe 64 GT/s SKP OS filtering
- Reference clock multiplier extended to 64 Gbd
- Notification of available software updates



## Table of Contents

Introduction .....	3
M8000 Series of BER Test Solutions .....	5
M8040A High-Performance BERT 64 Gbaud .....	5
Repeatable and Accurate Results with M8040A.....	7
Emulate Stress Conditions for NRZ and PAM4 Input Tolerance Testing with M8040A.....	8
Master PAM4 Receiver Test Challenges with M8040A.....	9
Real-Time Error Analysis for PAM4 and NRZ Signals .....	10
Automated Receiver Calibration and Characterization for IEE 802.3bs, IEEE 802.3ck, OIF-CEI-56G-VSR, PCI Express 4.0 and 5.0, USB 3.2, USB4 and TBT3 and TBT4 Interfaces .....	12
Specifications for M8045A and M8046A Modules and M8057A/B Remote Head .....	13
Specifications for Pattern Generator Module M8045A and Remote Head M8057A/B.....	14
Reference Clock Input (REF CLK IN).....	20
Jitter Specifications.....	24
External Level Interference (RI/SI) Sources .....	28
Emulate ISI (inter-symbol interference) with M8049A .....	29
Pattern Sequencer, Filler Symbol Filtering, and Interactive Link Training.....	30
Interactive Link Training for PCIe .....	32
Interactive Link Training for USB 3.2.....	33
Specifications Analyzer Module (Error Detector) M8046A .....	33
Error Analysis of PAM4 Signals Using an UXR-Series .....	41
User Interface and Remote Control.....	43
General Characteristics and Physical Dimensions.....	45
Remote Head M8057A/B.....	46
Specifications Assumptions .....	46
Ordering of M8040A High-performance BERT 64 Gbaud .....	47
Related Keysight Literature.....	50

## Introduction

The Keysight Technologies Inc. M8040A is a highly integrated BERT for physical layer characterization and compliance testing.

With support for pulse amplitude modulation 4-level, 3-level (PAM4, PAM3) and non-return-to-zero (NRZ) signals, and symbol rates up to 64 Gbaud (corresponds to 128 Gbit/s) it can be used for testing devices designed for 400/ 200 GbE, 800G, OIF CEI-56G and CEI-112G, PCIe ® 64/32/16/8/5 GT/s, USB 3.2, USB4, Thunderbolt™ 3 and Thunderbolt™ 4.

The M8040A BERT's true error analysis provides repeatable and accurate results, optimizing the performance margins of your devices.

## Key features

- Data rates from 2 to 32 and 64 Gbaud
- PAM4, PAM3 and NRZ selectable from user interface
- Built-in 5 tap transmitter FFE with multiple presets to compensate loss
- Integrated and calibrated jitter injection: RJ, LF and HF PJ (multi-tone, sinusoidal), BUJ, clk/2 jitter, sRJ, rSSC, and SSC (spread spectrum clocking)
- Forward Error Correction (FEC) encoding and error insertion for testing DUTs with FEC decoder
- Two pattern generator channels per module to emulate aggressor lane
- Linearity tests with adjustable PAM4 and PAM3 levels
- Interactive link training 2.5/5/8/16/ 32 GT/s PCI Express®
- Interactive link training for USB 3.2, 5 Gb/s and 10 Gb/s, x1 and x2
- SKP OS filtering for 2.5/ 5/ 8/ 16/ 32 64 GT/s PCI Express® and SKP OS filtering for USB 3.2
- ALIGN filtering for SATA 3G / 6G and SAS 3G / 6G/ 12G
- Short connections to the DUT with remote heads for the pattern generator
- True PAM4 error detection in real-time for low BER levels
- Built-in and adjustable equalization to re-open closed eyes
- Integrated clock recovery and control of external clock recovery units N1076A/B, N1077A, N1078A
- RI and SI level interference injection via M8054A interference source for M8194A/95A/96A AWG
- Graphical user interface and remote control via M8000 system software
- Error distribution analysis to debug burst error conditions
- Reference clock multiplier support with SSC extended to 64 Gbaud
- Scalable and upgradeable with options and modules

## Applications

The M8040A can be used for receiver (input) testing for many emerging interconnect standards, such as:

- IEEE 802.3bs 400 and 200 Gigabit Ethernet (200GAUI, 200GBASE, 400GAUI, 400GBASE)
- IEEE 802.3bj 100 Gigabit Ethernet
- IEEE 802.3cd 50, 100 and 200 Gigabit Ethernet
- IEEE 802.3ck 400 Gigabit Ethernet
- OIF CEI - 56G and -112G (NRZ and PAM4 versions)
- 25G PON
- PCI Express 64/32/16/8/5/2.5 GT/s
- CCIX
- SAS
- USB4
- USB 3.2
- Thunderbolt 3/4
- Universal Serial Bus USB 3.2, USB4 and USB4v2
- 64G/112G Fiber Channel
- InfiniBand-HDR
- Proprietary interfaces for chip-to-chip, chip-to-module, backplanes, repeaters, and active optical cables, operating up to 64 Gbaud.

## M8000 Series of BER Test Solutions

Simplified time-efficient testing is essential when you are developing next-generation computer, consumer, or communication devices

The Keysight M8000 Series is a highly integrated BER test solution for physical layer characterization, validation, and compliance testing.

With support for a wide range of data rates and standards, the M8000 Series provides accurate, reliable results that accelerate your insight into the performance margins of high-speed digital devices.



Figure 1. The M8000 Series BER test solution is highly integrated and scalable to address the test challenges of the next generation of high-speed digital receiver test.

The M8040A high-performance BERT 64 Gbaud extends the M8000 Series for 400G data center interconnect testing and PCIe 4/5, CCIX, SAS, USB 3.2, USB4 and TBT3/4 receiver characterization.

## M8040A High-Performance BERT 64 Gbaud

Simplifies accurate receiver characterization of devices operating up to 32 and 64 Gbaud with NRZ and PAM4 signals

Highest level of integration streamlines receiver test setups

With the M8040A, all critical test capabilities for input/receiver (RX) characterization are built-in. The pattern generator module provides calibrated and integrated jitter sources and de-emphasis to emulate the transmitter (TX) and to compensate for channel loss in the test setup. In addition, the M8040A provides an internal clock synthesizer and a second pattern generator output channel to emulate an aggressor lane.

The analyzer provides true PAM4 and NRZ error analysis in real time and full sampling to measure down to very low BER and SER.

This high level of integration with the M8040A makes the receiver test set-up connections easier and more robust. Setup and debug time are shortened, calibration is simpler, and the frequency of re-adjustments is reduced, resulting in a more efficient use of overall test time.

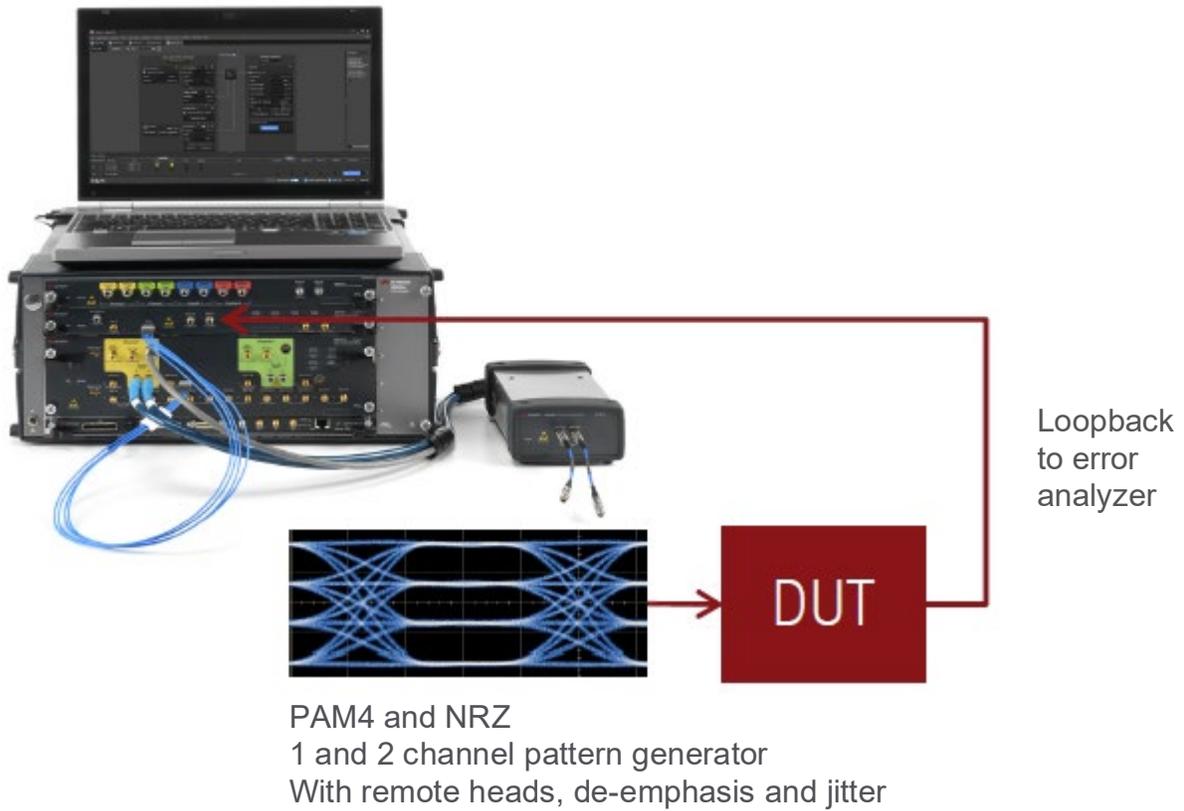


Figure 2. The M8040A streamlines complex receiver test setups. Each of the 1 or 2 pattern generator channels provides built-in de-emphasis, jitter sources, and a remote head to reduce the distance between the generator output and the DUT test board. The full sampling error analyzer can detect errors in real-time for NRZ and PAM4 signals without the need to split up the PAM4 signal for multiple error detector channels

## Repeatable and Accurate Results with M8040A

The M8040A high-performance BERT provides clean NRZ and PAM4 signals up to 64 Gbaud with fast transitions and low intrinsic jitter. The remote head concept of M8040A with the short 1.85 mm cables brings the performance close to the device under test, minimizing signal degradations caused by lossy channels.



Figure 3. The remote head M8057A/B is required for each channel and is required for NRZ and PAM4 signals. It contains an adjustable gain amplifier without re-timer. Users can select NRZ or PAM4 coding and de-emphasis taps settings from the user interface with no need to reconnect cables. The cable between the remote head and the module is 0.85 m long. This allows positioning the remote head closely to the test board for the device under test.

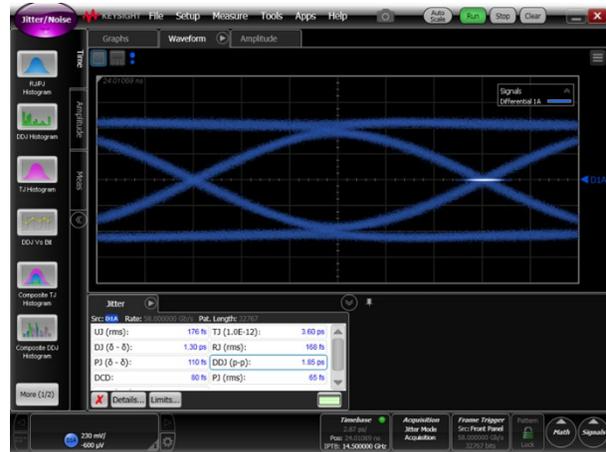


Figure 5. Clean 58 Gbaud NRZ output signal of pattern generator module M8045A with remote head M8057B using the internal clock source with 600 mV output amplitude and PRBS  $2^{15}-1$ . Measured with Infiniium DCA-X 86100D with N1045A and manual de-emphasis adjustment.

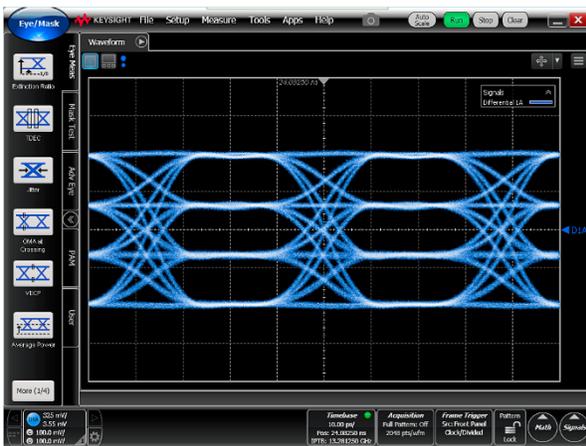


Figure 4. Clean 26.5625 Gbaud PAM4 output signal of pattern generator module M8045A with remote head M8057B using the internal clock source with 600 mV output amplitude and PRBS  $2^{15}-1$ . Measured with Infiniium DCA-X 86100D and N1045A and manual de-emphasis adjustment.

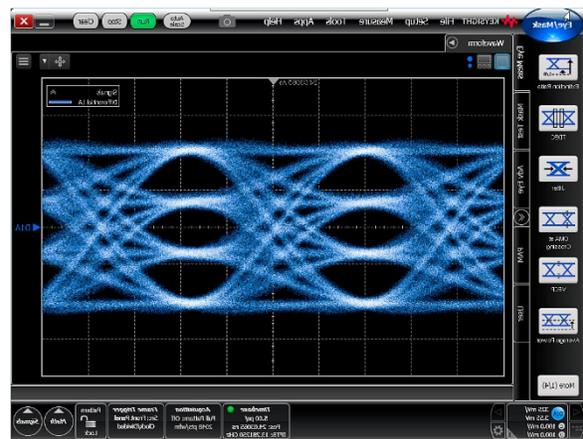
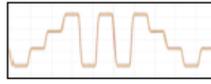


Figure 6. Clean 53.125 Gbaud PAM4 output signal of pattern generator module M8045A with remote head M8057B using the internal clock source with 600 mV output amplitude and PRBS  $2^{15}-1$ . Measured with Infiniium DCA-X 86100D and N1045A and manual de-emphasis adjustment.

## Emulate Stress Conditions for NRZ, PAM3 and PAM4 Input Tolerance Testing with M8040A

M8040A provides all capabilities required for input tolerance test:

- 1 or 2 channels. Second channel can be used as aggressor lane to emulate crosstalk effects
- Data rates are adjustable from 2 Gb/s NRZ up to 64 Gbaud PAM3 or PAM4, selectable NRZ or PAM4 or PAM3
- Algorithmic PRBS, QPRBS, PRTS and memory-based patterns, pattern sequencer with loops, error injection at the bit level (NRZ patterns) and at the symbol level (PAM3 and PAM4 patterns)
- Generates FEC encoded patterns with pre-coder on 1 lane to test DUTs with FEC decoder
- Built-in and calibrated jitter sources that can be used simultaneously: random jitter (RJ), multi-UI low-frequency jitter, multi-tone high-frequency jitter, BUJ, clk/2 jitter, spread-spectrum clocking (SSC), residual SSC (rSSC), spectrally distributed RJ (sRJ)
- Lock system clock to an external reference clock with a multiplying PLL
- De-emphasis for pre- and post-cursor to emulate transmitter de-emphasis and compensate for loss in the test setup
- Inject random interference (RI) and sinusoidal interference (SI) by couplers. The M8000 software controls M8054A, AWG M8195A and M8196A as RI/SI source or as aggressor lanes
- Automated jitter tolerance testing

	NRZ	PAM4
		
Effective data rate	Bit rate	Symbol rate
32 Gbit/s	32 Gbit/s	16 Gbaud
64 Gbit/s	64 Gbit/s	32 Gbaud
128 Gbit/s	128 Gbit/s	64 Gbaud

Covered by  
M8040A

Related IEEE802.3cd 50/100/200GBASE/GAUI proposed symbol rate * # of lanes	Related IEEE802.3bs 200GBASE/200GAUI symbol rate # of lanes	Related IEEE802.3bs 400GBASE/400GAUI symbol rate # of lanes	Related OIF CEI-56G symbol rates
25.78125 Gb/s Gb/s NRZ * 1 lane	26.5625 Gbit/s NRZ * 8 lanes	26.5625 Gbit/s NRZ * 16 lanes	
26.5625 Gbaud PAM4 * 1/2/4 lanes 53.125 Gbaud PAM4 * 1/2 lanes	26.5625 Gbaud PAM4 * 4 lanes	26.5625 Gbaud PAM4 * 8 lanes 53.125 Gbit/s NRZ * 8 lanes	LR-PAM4: 19.6 to 30 Gbaud MR-PAM4: 18 to 29 Gbaud MR-NRZ: 39 to 56.2 Gbit/s VSR-PAM4: 18 to 29 Gbaud VSR-NRZ: 39 to 56.2 Gbit/s XSR-PAM4: 18 to 29 Gbaud XSR-NRZ: 39.8 to 58 Gbit/s USR-NRZ: 19.6 to 58.0 Gbit/s

Figure 7. M8040A supports data rates up to 32 Gb/s NRZ, 64 Gb/s NRZ, 32 Gbaud PAM4 and 64 Gbaud PAM4. The user interface allows selection of NRZ and PAM4 without reconnecting the BERT test setup.

## Master PAM4 Receiver Test Challenges with M8040A

Design and test engineers who need to characterize devices that support PAM4 data formats are facing new test challenges in addition to the signal integrity issues known from 25 Gb/s NRZ device testing.

For PAM4 input receiver tolerance test, this means impairments that may occur in the real-world should be tolerated by the receiver under test without exceeding the desired BER level. Typical receiver tests include jitter tolerance, interference tolerance test and level sensitivity margins that are applicable for NRZ and PAM4 devices. In addition, PAM4 receivers require additional margin testing for level non-linearity, cross-talk effects from adjacent lanes and vertical eye closure.



Figure 8. PAM4 eyes can show a level separation mismatch. Receivers must be able to detect the digital signal content properly within the given mismatch ratio.

## Real-Time Error Analysis for PAM4 and NRZ Signals

Receiver verification checks if the receiver under test operates below the specified BER while emulating the worst-case transmitter and channel conditions. BER measurements are well established for NRZ signals by using a traditional BERT, but what does this mean for PAM4 signals?

For proper error detection of PAM4 signals, all thresholds ( $V_{low}$ ,  $V_{mid}$ , and  $V_{upper}$ ) have to be analyzed simultaneously to ensure a correct symbol error measurement (see Figure 9). If a “1” is detected at the  $V_{mid}$  threshold, the received pattern can have level 2 or 3. Only if the level detected at  $V_{upp}$  is checked simultaneously with  $V_{mid}$ , it can be determined if the received inputs have the correct level for a 2 or a 3. If two thresholds are errored within one UI, this case translates just into one symbol error.

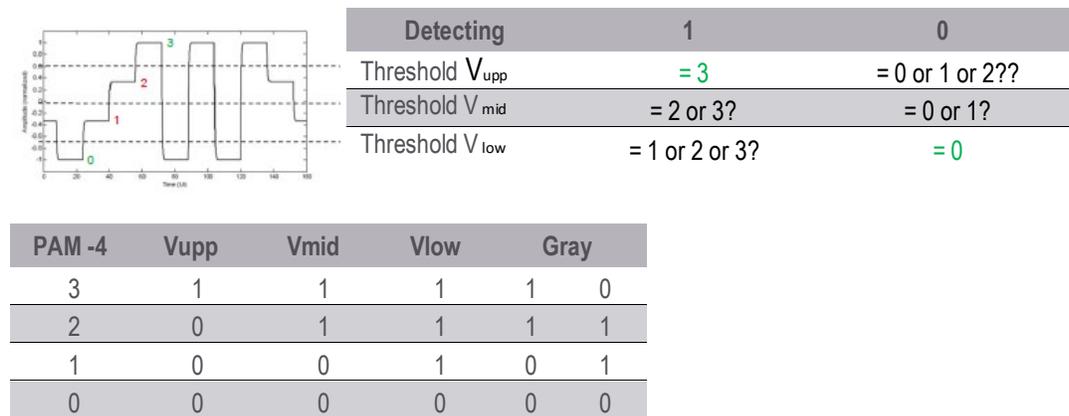


Figure 9. Only a true PAM4 error analyzer like M8040A, can provide a PAM4 symbol error rate in real-time without post-processing. Error ratios down to  $10^{-15}$  or error-free can be measured even for long PRBS  $2^{31}-1$ , SSPRQ, QPRBS13-CEI or QPRBS31-CEI patterns. Errored 0,1,2,3 and symbol errors can be counted separately for further debugging.

- The M8040A provides real-time error analysis of PAM4 and NRZ signals.
- Key capabilities of the error analyzer module M8046A include:
  - One differential channel per analyzer module
  - Symbol rates from 5 to 30 Gbaud for PAM4 and from 5 to 32 and 64 Gb/s for NRZ
  - Native PAM4 decoding
  - Built-in equalization to re-open closed eyes at the analyzer input
  - Selectable expected patterns like QPRBS31, SSPRQ, pattern memory, pattern sequencing, masking, Gray coding and custom PAM4 symbol mapping
- Integrated clock recovery option and control via M8070ADVB of external clock recovery units N1076A/B, N1077A, N1078A
- DUT control interface allows to access built-error counters from the M8070ADVB advanced measurement software package.
- Can be used in combination with M8045A pattern generator or AWGs M8195/6/4A

## Error distribution analysis

The Error Distribution Analysis M8070EDAB offers burst error analysis, frame loss ratio estimation and error mapping. Following metrics are calculated for user-definable symbol length, frame length and correctable symbol errors per frame:

- Symbol-error per frame distribution with user-definable symbol and frame length
- Consecutive error distance distribution
- Frame loss ratio, counted and estimated
- Error map provides insight into burst error mechanisms.

The M8070EDAB is a licensed software package that requires a M8070B version 6.0 and higher.

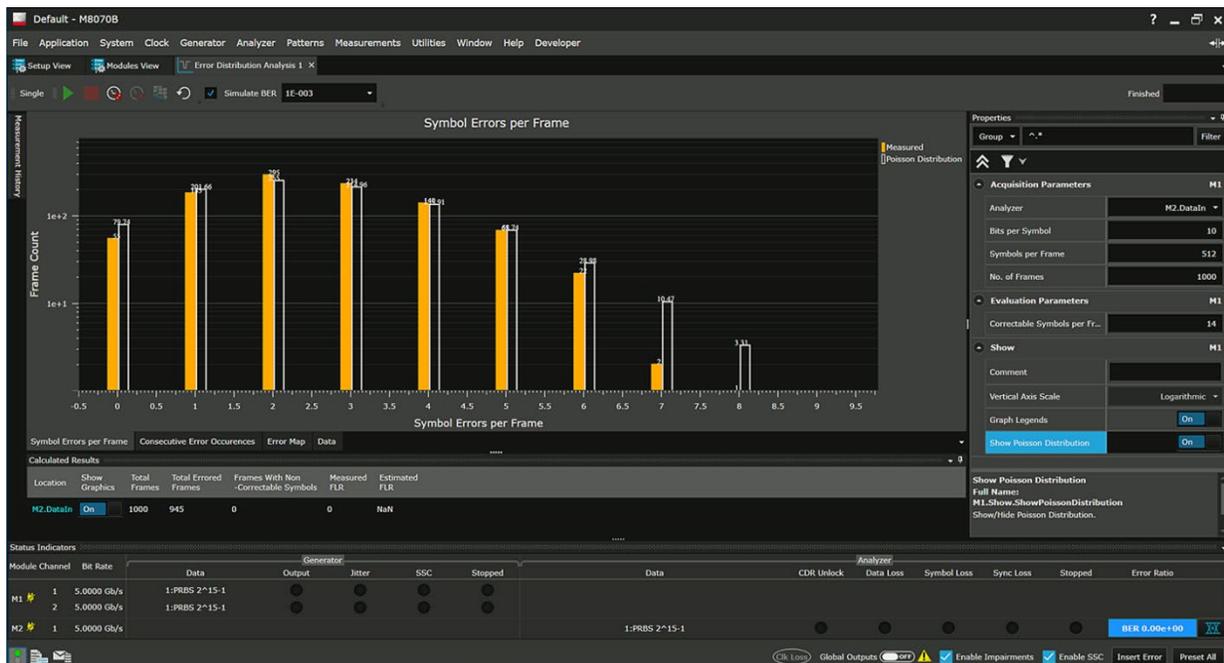


Figure 10. The error distribution analysis M8070EDAB provides multiple views to debug the error distribution. The figure shows an example of symbol errors per frame based on captured pattern streams, with the measured frame loss ratio, based on user-definable number of bits per symbol, correctable symbols per frame and frame length.

# Automated Receiver Calibration and Characterization for IEEE 802.3bs, IEEE 802.3ck, OIF-CEI-56G-VSR, PCI Express 4.0 and 5.0, USB 3.2, USB4 and TBT3 and TBT4 Interfaces

To simplify the compliance testing and characterization of receiver test, Keysight provides automated receiver test automation software for various electrical and optical interface standards. Here is an overview of test automation software solutions available supporting the M8040A high-performance BERT.

Standard	Interface	Variants	BERT	Test Automation Software
IEEE 802.3bs	Electrical, Chip-to-module	400GAUI 200GAUI	M8040A	M8091BSPA Pre-Compliance Receiver Test Automation for IEEE 802.3bs
IEEE 802.3bs	Optical	400GBASE-LR8/-FR8 and 200GBASE-LR4/-FR4/-DR4	M8040A	N4917BSCA Optical Receiver Stress Test Solution
IEEE 802.3ck	Electrical	Chip-to-chip, Chip-to-module	M8040A	M8091CKPA Pre-compliance Receiver Test Automation for IEEE 802.3ck, draft 1.2
OIF CEI 4.0	Electrical, host and module	56G-VSR,-MR, -LR PAM4	M8040A	M809256PB Pre-Compliance Receiver Test Automation for CEI-56G
PCI Express 4.0	Electrical	PCIe 8/16 GT/s	M8040A	N5991PB4A Receiver Test Automation for PCIe 4.0 base specification N5991PC4A Receiver Test Automation for PCIe 4.0 PHY Test Specification for CEM N5991PA3A-ADD Automated LinkEQ RX and TX testing
PCI Express 5.0	Electrical	PCIe 8/16/32 GT/s	M8040A	N5991PB5A Receiver Test Automation for PCIe 5.0 base specification N5991PC5A Receiver Test Automation for PCIe 5.0 PHY Test Specification for CEM N5991PA3A-ADD Automated LinkEQ RX and TX testing
SAS	Electrical	SAS 12 and 24 Gb/s	M8040A	N5991SA4A Receiver Test Automation for SAS
SATA	Electrical	SATA 3	M8040A	N5991ST3A Receiver Test Automation for SATA
CCIX	Electrical	CCIX 20 and 25 GT/s	M8040A	N5991C25A Receiver Test Automation for CCIX
USB 3.2	Electrical	USB 3.2	M8040A	N5991U32A Receiver Test Automation for USB 3.2
USB4	Electrical	USB4	M8040A	N5991U40A Receiver Test Automation for USB4, TBT4 and TBT3
TBT	Electrical	Thunderbolt 3/4	M8040A	N5991U40A Receiver Test Automation for USB4, TBT4 and TBT3

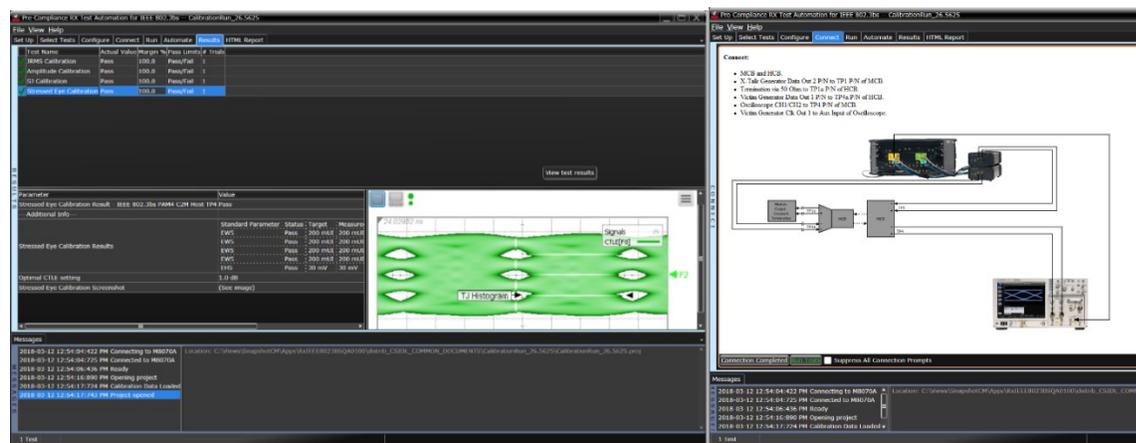


Figure 11. Automate the complicated stress signal calibration procedure with guided steps how to connect the test setup and pre-compliance measurements by using the M8091BSPA receiver test automation software for IEEE 802.3bs for chip-to-module interfaces 400GAUI-8 and 200GAUI-4. The figure shows screen shots of the automation software with the results of a successful stress calibration (left side) and guided test setup (right side).

## Specifications for M8045A and M8046A Modules and M8057A/B Remote Head

M8045A pattern generator module for two data channels, 3-slot AXIe



M8045A pattern generator module for one data channel, 3-slot AXIe



M8057A/B remote head with cable connections (0.85 m) front and rear view



M8046A analyzer module, 1-slot AXIe



Figure 12. Front panel views of pattern generator module M8045A (top) as 2 and 1 channel (center) versions, remote head M8057A/B, and error analyzer module M8046A (bottom). To allow a very short connection to the device under test, the remote head is used. One remote head is needed for each of the pattern generator data outputs of M8045A.

# Specifications for Pattern Generator Module M8045A and Remote Head M8057A/B

## Data output (DAT OUT 1, DATA OUT 2)

The pattern generator supports symbol rates up to 32 Gbaud or 64 Gbaud, default is one channel and NRZ format.

The remote head M8057A/B is needed once per channel. Using the P and N outputs of the M8045A without remote head is prohibited.

For the following generator functions a separate module option is required:

- PAM4 coding up to 32 Gbaud (M8045A Option 0P3)
- PAM4 extension to 64 Gbaud (M8045A Option 0P6)
- Second data channel (M8045A Option 0G2)
- Advanced jitter sources (M8045A Option 0G3)
- De-emphasis (M8045A Option 0G4)
- Reference clock multiplier with bandwidth 2/5 MHz (M8045A Option 0G6)
- Forward Error Correction (FEC) encoding (M8045A Option 0G9)

**Table 1. Data output characteristics for M8045A with remote head M8057A/B.**

All timing parameters re measured @ 0.5 V into ground at data outputs of remote head M8057A/B	
Symbol rate	2.025 to 32.4 Gbaud for M8045A Option -G32 2.025 to 58.0 Gbaud (all specifications are valid up to 58 Gbaud with over-programming up to 64.8 Gbaud) for M8045A Option -G64
Data format	NRZ (default) PAM4 (requires M8045A Option -0P3 and for symbol rates above 32 Gbaud -0P6 in addition) PAM3 (requires M8045A Option -0P3)
Channels per module	1 or 2 (requires M8045A Option -0G2 and second remote head)
Amplitude with M8057B for symbol rates < 58 Gbaud	80 mV to 0.9 Vpp single ended 160 mV to 1.8 Vpp differential
Amplitude with M8057A For symbol rates < 32.4 Gbaud	50 mV to 0.9 Vpp single ended 100 mV to 1.8 Vpp differential
For symbol rates < 58 Gbaud	50 mV to 0.6 Vpp single ended 100 mV to 1.2 Vpp differential
Amplitude accuracy	$\pm 10\%$ $\pm 10$ mV typical (AC) <sup>1</sup>
Output voltage window	-1 to +3.0 V depends on external termination voltage <sup>5</sup>
External termination voltage	-1 to +3.0 V
Offset accuracy	25 mV +10% of offset +1% of amplitude. The offset is defined as $0.5 * (HIL+LOL)$ . See <sup>5</sup>
Transition time <sup>2</sup>	9 ps typical (20 to 80%) for symbol rates > 32.4 Gbaud 11 ps typical (20%-80%) for symbol rates $\leq$ 32.4 Gbaud
Intrinsic total jitter	8 ps typical @ 32.0 Gb/s NRZ, PRBS 15, BER $10^{-12}$
Intrinsic random jitter (NRZ)	5 mUI rms typical @ symbol rates between 2.025 Gbaud and < 22 Gbaud 7 mUI rms typical @ symbol rates between 22 Gbaud and < 32.4 Gbaud 10 mUI rms typical @ symbol rates between 32.4 Gbaud and < 40 Gbaud 12 mUI rms typical @ symbol rates between 40 Gbaud and < 52 Gbaud 10 mUI rms typical @ symbol rates between 52 Gbaud and < 58 Gbaud

**Table 1. Data output characteristics for M8045A with remote head M8057A/B. (continued)**

Data delay range	0 to 10 ns, resolution 100 fs
Data delay accuracy	$\pm$ (max. (1.5 ps or 10 mUI whatever is higher) + 1% of entered value) typical <sup>3</sup>
Electrical idle	The output transitions from full swing to 0 V amplitude and vice versa at constant offset within 1 UI.
Skew between normal and complement output	3 ps maximum at the end of the recommended cable pair. Fixed.
Skew between data output ch 1 and data output ch 2	370 ps maximum <sup>4</sup> Repeatability after manual de-skew $\pm$ 300 ps typical
Termination impedance range	To protect the output stage, the output is disabled when an unexpected voltage or termination impedance is detected. DC output coupling mode: Termination range for devices connected to data out: <ul style="list-style-type: none"> <li>• Unbalanced 50 <math>\Omega</math> +15 <math>\Omega</math> / -10 <math>\Omega</math></li> <li>• Typical balanced 100 <math>\Omega</math> <math>\pm</math>30 <math>\Omega</math> typical</li> </ul> Operation into open <sup>7</sup> is possible for following ranges when DC coupled and balanced termination modes are selected: <ul style="list-style-type: none"> <li>• Output amplitude max. 450 mV</li> <li>• Offset 0 to 370 mV</li> </ul>
Termination modes	Balanced/ unbalanced
Coupling	DC/ AC selectable coupling of device under test
Connectors	1.85 mm, female

1. At 5 Gbaud measured with DCA-X N1045A and clock pattern and in the middle of the eye
2. Measured with DCA-X N1045A
3. At constant temperature
4. Requires M8070A software revision 4.5 or M8070B SW 6.0 or later and a module serial number above DE56C00400
5. High level voltage range=  $2/3 * V_{term} - 0.95 \text{ V} < \text{HIL} < V_{term} + 2 \text{ V}$
6. Low level voltage range=  $2/3 * V_{term} - 1 \text{ V} < \text{LOL} < V_{term} + 1.95 \text{ V}$
7. Available with M8070B SW 7.5 and higher

## De-emphasis (DATA OUT)

The M8045A provides built-in de-emphasis with positive and negative cursors based on a finite impulse response (FIR) filter see figure 11. Users can enter the de-emphasis in coefficient values. The M8045A supports five de-emphasis cursors with an adjustable main-cursor position between cursor 1 and cursor 3. Pre-requisite to use the adjustable main cursor is M8070B software revision 7.1 or later. This allows selecting the following configuration

Main cursor position	Number of pre-cursors	Number of post-cursors
1	1	3
2	2	2
3	3	1

**Table 2. Specifications for multi-tap de-emphasis (requires Option 0G4).**

	NRZ	PAM4
De-emphasis taps	5, can be adjusted for each channel independently	
Coefficient c0	0.0 to $\pm 0.40^1$	0.0 to $\pm 0.40^1$
Coefficient c1	0.0 to $\pm 0.40^1$	0.0 to $\pm 0.40^1$
Coefficient c2	0.0 to $\pm 1.0^1$	0.0 to $\pm 1.0^1$
Coefficient c3	0.0 to $\pm 0.40^1$	0.0 to $\pm 0.40^1$
Coefficient c4 <sup>2</sup>	0.0 to $\pm 0.40^1$	0.0 to $\pm 0.40^1$
Cursor coefficient resolution	0.01	0.01
Tap optimization	Auto-optimization of DE taps is possible when using DCA and M8070ADVB	

1. Sum of all cursors absolute values may not exceed 1.0  $|c0|+|c1|+|c2|+|c3|+|c4| \leq 1$ . Also,  $|c0|, |c1|, |c3|, |c4| < |c2|$ .
2. Requires M8070A software 5.0 or M8070B SW 6.0 or later.

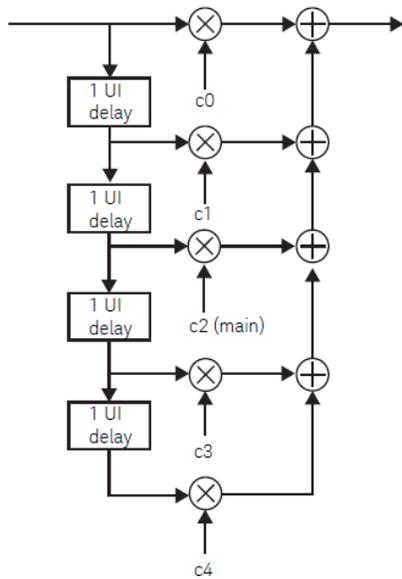


Figure 13. The pattern generator of M8045A provides integrated de-emphasis to emulate TX equalization. The example shows a configuration with two post-cursors c3 and c4, the main cursor c2 and two pre-cursors c0 and c1.

## De-emphasis presets for PCIe testing

If PHY protocol mode PCIe3, PCIe4 or PCIe 5 for the pattern generator sequence is selected the de-emphasis capabilities are switched from the multi-tap FIR to a PCI Express type of FIR editor with coefficient entry as integers dependent of the selected full swing. A full swing from 24 to 63 coefficient resolution steps can be selected.

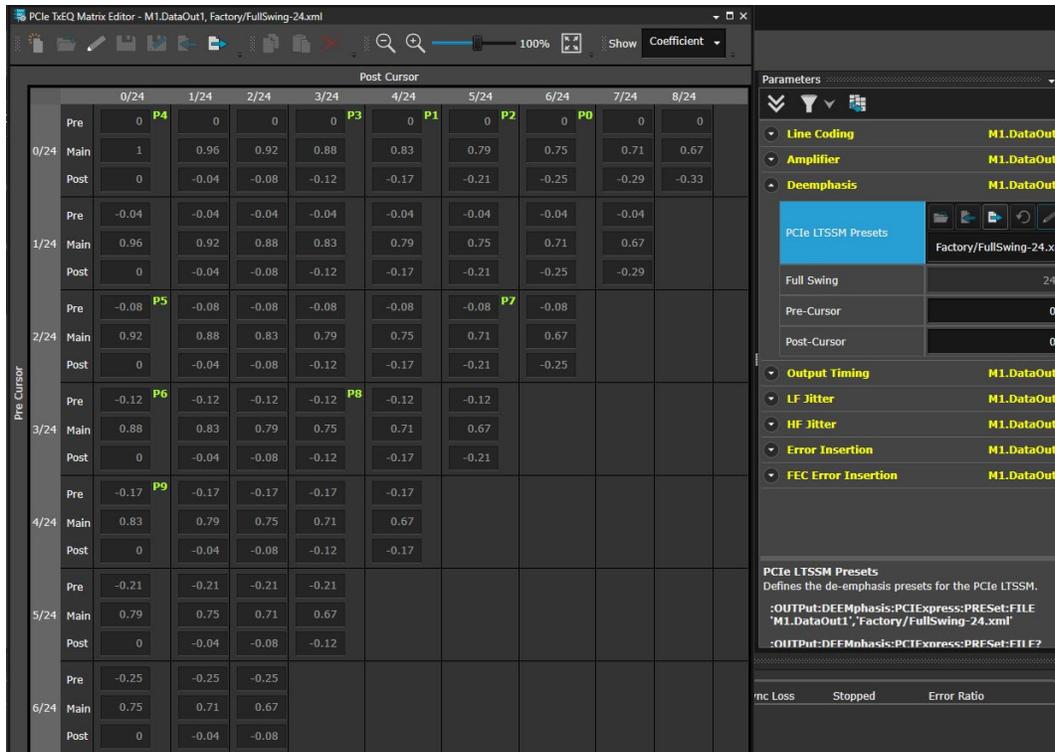


Figure 14. The TxEQ matrix editor can be accessed if the PHY protocol mode PCIe 3, PCIe 4 or PCIe 5 is selected for the pattern generator sequence.

## Forward Error Correction (FEC) encoding (DATA OUT)

The M8045A pattern generator module supports forward error correction (FEC) and precoding encoding according to IEEE802.3cd.

Users can inject pre- and post-FEC errors to test the DUT's devices FEC decoder function.

**Table 3. Specifications for FEC (Forward Error Correction) encoding (requires M8045A Option 0G9).**

FEC encoding	50GBASE-R, 100GBASE-R, 200GBASE-R (PCS 0,1), 400GBASE-R (PCS 0,1)
Reed-Solomon Code	RS (544,514)
Scrambler	PRBS $2^{58}-1$
Pattern sequence	These patterns form pattern library can be FEC encoded: Remote faults, Scrambled idle
Line coding	PAM4
Number of lanes	1
Symbol rate	26.5625 Gbd PAM4
FEC error injection	For 50GBASE-R: Pre-FEC: insertion of a single BIP Post-FEC: FEC symbol errors, randomly distributed, selectable amount of symbol errors per FEC frame
Pre-coder	PAM4: $1/(1+D) \bmod 4$ , can be switched on/off. Follows IEEE802.3 Clause 135.5.7.2. for PAM4 encoded lanes.
Synchronization to A400GE-DD	Yes, requires trigger and reference clock connection. Requires M8045A-0G9 and M8070B 7.0 or later.
Pre-requisites	M8045A with option 0P3 and 0G9, M8070A SW 5.1/ M8070B 6.7 or later.

## Clock output 1 and 2 (Channel 1 CLK OUT, channel 2 CLK OUT)

These clock output provide two modes. They can operate with the same jitter as the corresponding data output or operate in a clean mode.

**Table 4. Specifications for channel 1 clock output and channel 2 clock output.**

FEC encoding		1.0125 to 16.2 GHz with M8045A-G32 1.0125 to 32.4 GHz with M8045A-G64
Frequency divider factors		Symbol rate / clock divider: 2, 4, 8, 16. Divided output frequency must fit into frequency range
Clean clock mode	On	No jitter injection, no SSC
	Off	Same jitter and SSC as data output of same channel
Amplitude		1 V typical nominal single ended
Duty cycle		50%, accuracy $\pm$ 15% typical
Intrinsic random jitter		6 mUI rms typical for symbol rates between 2.025 Gbaud and $\leq$ 27 Gbaud 10 mUI rms typical for symbol rates $>$ 27 Gbaud. Refers to mUI of symbol rate.
Termination		50 $\Omega$ into GND or external termination voltage. Do not operate into open.
Coupling		AC coupled. Single ended.
Connectors		3.5 mm, female

## Clock output (CLK OUT)

This is a differential clock output with many sub-rate clock dividers. LF SJ and HF jitter can be turned off and on individually. HF jitter has the same setting as HF jitter of data output of channel 1. Delay on the trigger output also impacts clock output.

**Table 5. Clock output specifications.**

CLK frequency range	2.025 to 16.20 GHz	
Clock divider in relation to clock frequency range	n * (1, 2, 4, 8, 10, 16, 20, 24, 30, 32, 40, 50, 64, 66, 80) with n= 1 < 16.2 GHz n= 2 for 16.2 GHz to 32.4 GHz n= 4 > 32.4 GHz For other dividers use TRIG OUT	
Frequency resolution	1 Hz	
Frequency accuracy	± 15 ppm	
Amplitude	Differential	0.2 to 2.0 V, 10 mV steps
	Single ended	0.1 to 1 V, 5 mV steps
Output voltage window	-1 to +3 V <sup>1</sup>	
External termination voltage	-1 to +3 V	
Transition times	20 ps typical (20 to 80%)	
Duty cycle	50%, accuracy ± 15%	
Clock modes	See Table 6	
Intrinsic random jitter	300 fs rms typical at 16.2 GHz and clock divider = 1	
Jitter injection	LF Jitter: <ul style="list-style-type: none"> <li>• Can be set independently from Data Out</li> <li>• Has the same LF jitter parameters and ranges as Data Out</li> </ul> HF Jitter: <ul style="list-style-type: none"> <li>• On -&gt; the jitter values from Data Out1 HF Jitter are applied to Clock Out</li> <li>• Off -&gt; no HF Jitter</li> </ul> SSC: <ul style="list-style-type: none"> <li>• SSC is a system-wide parameter and therefore applies to CLK OUT too</li> </ul>	
SSB phase noise <sup>2</sup>	- 85 dBc/ Hz typical at 10 kHz offset and internal clock and 10/100 MHz as external reference clock - 80 dBc/Hz typical with 10 kHz offset for reference clock multiplier bandwidth 0.1 MHz	
Termination	50 Ω into GND or external termination voltage. Do not operate into open. Unused outputs must be terminated into termination voltage	
Coupling	DC coupled, differential	
Connectors	3.5 mm, female	

1. If Vterm is other than 0 V the following applies:  
 High level voltage range=  $2/3 * V_{term} - 0.95 \text{ V} < \text{HIL} < V_{term} + 2 \text{ V}$   
 Low level voltage range=  $2/3 * V_{term} - 1 \text{ V} < \text{LOL} < V_{term} + 1.95 \text{ V}$
2. For reference clock multipliers < 400.

**Table 6. Clock modes.**

	Clock generation	Input frequency range
Internal	PLL with internal reference	N/A
Reference	PLL with bandwidth below 1 kHz	10/100 MHz
Direct	No PLL. Maximum symbol rate is 16.2 Gbaud	8.1 to 16.2 GHz
Reference clock multiplier bandwidth 100 kHz	m/n PLL with loop bandwidth 100 kHz m, n = 1 to 1620	10 MHz to 16.2 GHz

## Reference Clock Input (REF CLK IN)

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator. It also allows using an external clock, see clock modes as shown in table 6. A SSC tolerant PLL is used to multiply the external reference clock to the system clock.

**Table 7. Reference clock input specifications (M8045A only).**

Input amplitude	0.2 to 1.4 Vpp
Input frequency	10 MHz to 16.2 GHz, depends on clock mode and max. data rate option <sup>1</sup>
Interface	Single ended. 50 Ω nominal
Connector	SMA, female

1. A minimal slew rate of 0.3 V/ns at the REF CLK IN signal is required to ensure a proper frequency measurement. If this requirement can't be met the input frequency should be set manually

**Table 8. Predefined settings for reference clock multiplier (M8045A with Option OG6 only).**

Ref clock input	Standard	Target data rate	Multiplier	PLL loop BW
100 MHz	PCIe *	32 Gbd (NRZ or PAM4)	320	2 MHz
100 MHz	PCIe	16 Gb/s	160	2 MHz
100 MHz	PCIe	8 Gb/s	80	5 MHz
100 MHz	PCIe	5 Gb/s	50	5 MHz
100 MHz	PCIe	2.5 Gb/s	25	5 MHz
100 MHz	USB4 Gen2	10 Gb/s	100	5 MHz
100 MHz	USB4 Gen3	20 Gb/s	200	5 MHz
103.125 MHz	TBT3 Gen2	10.3125 Gb/s	100	5 MHz
103.125 MHz	TBT3 Gen3	20.625 Gb/s	200	5 MHz
19.2 MHz	MIPI M-PHY	2.496/2.9184/4.992/5.8368/ 9.984/11.6736 Gb/s	130/152/260/304/520/608	2 MHz
26 MHz	MIPI M-PHY	2.496/2.912/4.992/5.824/ 9.984/11.648 Gb/s	96/112/192/224/384/448	2 MHz
38.4 MHz	MIPI M-PHY	2.496/ 2.9184/ 4.992/ 5.8368/ 9.984/ 11.6736 Gb/s	65/76/130/152/260/304	2 MHz
52 MHz	MIPI M-PHY	2.496/2.912/4.992/5.824 9.984/11.648 Gb/s	48/56/96/112/192/224	2 MHz
Pre-requisites	Requires M8045A with a serial number above MYxxx1000 and M8070B software revision 6.5 or later. Older serial numbers can be upgraded (M8045A-UR4, Return-to-Keysight).			

1. Requires M8070B SW 8.0 or later

## Trigger output (TRG OUT)

This output is used to send a trigger signal to another connected device, such as an oscilloscope. Also it can be used to generate a sub-rate clock. The trigger output can be used in different modes:

1. Divided clock, dividers:
  - a. For <16.2 Gbaud trigger data rate range 2 to 65532
  - b. For 16.2 to 32.4 Gbaud trigger data rate range 4 to 65532 with step resolution of 2
  - c. For > 32.4 Gbaud trigger output data range 8 to 65532 with step resolution of 4

2. Sequence block trigger with adjustable pulse width and offset
3. PRBS sequence trigger with adjustable pulse width

**Table 9. Trigger output specifications.**

Amplitude	single-ended	0.1 to 1.0 Vpp
	differential	0.2 to 2.0 Vpp
Jitter injection	The injected jitter is always the same as the jitter at the CLOCK OUT	
Delay range	0 to 100 ns, resolution 100 fs	
Delay accuracy	± (max. (1.5 ps or 10 mUI whatever is higher) + 1 % of entered value) typical <sup>3</sup>	
Skew between trigger output and data output ch 1 or ch 2, <sup>2 3 4</sup>	370 ps maximum	
	Repeatability after manual deskew ± 250 ps typical	
Output voltage window	-1 to 3 V <sup>1</sup>	
External termination voltage	-1 to 3 V	
Interface	Differential, 50 Ω	
Connector	3.5 mm, female	

1. If V term is other than 0 V the following applies:  
High level voltage range=  $2/3 * V_{term} - 0.95 \text{ V} < \text{HIL} < V_{term} + 2 \text{ V}$   
Low level voltage range=  $2/3 * V_{term} - 1 \text{ V} < \text{LOL} < V_{term} + 1.95 \text{ V}$
2. Requires M8070A software 4.5 or M8070B SW 6.0 or later and a module serial number above DE56C00400
3. At constant temperature
4. Sequencer controlled trigger (use a cable with 3.75 ns delay (~ 865 mm) connected to trigger output)

## Reference clock output (REF CLK OUT)

Outputs a 10 and 100 MHz clock, 1 Vpp single ended into 50 Ω

Connector: SMA, female

## Control input A and B (CTRL IN A, CTRL IN B)

Functionality of each input can be selected as: sequence trigger, error addition.

**Table 10. Control input specifications.**

Input voltage	-1 V to +3 V
Termination voltage	-1 V to +3 V
Termination voltage accuracy	$\pm (25 \text{ mV} + 1\%)$
Threshold voltage	-1 V to +3 V
Delay to data output	< 1 ms, Repeatability $\pm 512 \text{ UI}$ (requires M8070A software 4.5/ M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	3.5 mm, female

## Control output A and B (CTRL OUT A, CTRL OUT B)

Generates a pulse or static high/low if used from sequencer.

**Table 11. Control output specifications.**

Amplitude <sup>1</sup>	0.1 V to +2 V
Output voltage <sup>1</sup>	-0.5 to 1.75 V
Delay to data output	$\pm 512 \text{ UI} \pm \text{jitter amplitude}/2$ (requires M8070A software 4.5/ M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	3.5 mm, female

1. When terminated with 50  $\Omega$  into GND. Doubles into open.

## Connection Link A and B (LINK 1234)

This communication link enables interactive link training with low latency between a M8045A pattern generator channel and a M8046A analyzer module. Requires using cable M8051A-801 and M8045A with a serial number of MY/DExxx1000 or higher. Older serial numbers can be upgraded (M8045A-UR4, Return-to-Keysight).

## Synchronization out (SYNC OUT)

The sync output is a clock output to synchronize additional modules to a common clock. Can be used to synchronize the M8046A with the system internal clock.

## System input A/B (SYS IN A/B)

These are control inputs to synchronize events for the pattern sequencer.

**Table 12. System input specifications.**

Input voltage	-1 V to +3 V
Termination voltage	-1 V to +3 V
Threshold voltage	-1 V to +3 V
Delay to data output	< 1 ms, Repeatability $\pm 512$ UI. (requires M8070A software 4.5 or M8070B SW 6.0 or later and a module serial number above MY/ DE56C00400)
Connector	SMA, female

## System output A/B (SYS OUT A/B)

Generates a pulse or static high/low controlled by the pattern sequencer. A and B outputs are independently controllable.

**Table 13. System output specifications**

Amplitude <sup>1</sup>	0.1 V to 2 V
Output voltage <sup>1</sup>	-0.5 to 1.75 V
Delay to data output	$\pm 512$ UI $\pm$ jitter amplitude/2 (requires M8070A software 4.5/M8070B SW 6.0 or later and a module serial number above DE56C00400)
Connector	SMA, female

1. When terminated with 50  $\Omega$  into GND. Doubles into open.

## Auxiliary input (AUX IN)

Not used.

## Clock input (CLK IN)

For future use. See reference clock input for direct clock mode.

## Jitter Specifications

The M8045A has integrated and calibrated jitter sources. To use the jitter injection the M8045A Option -0G3 is required.

**Table 14. Specifications for low frequency periodic jitter (requires Option -0G3 advanced jitter sources).**

Low frequency periodic Jitter (LF PJ) (generated by IQ modulator)	Amplitude range	0 to 123.5 UI * symbol rate (in Gbaud) for modulation frequencies of 100 Hz to 10 kHz, see table below. For modulation frequencies between 10 kHz and 40 MHz the maximum  LF PJ = $\frac{7.792 \text{ UI} * 10^{-3} * \text{symbol rate}}{\text{modulation frequency}^{1,2}}$
	Frequency	100 Hz to 40 MHz, sinusoidal modulation
	Jitter amplitude	$\pm 2\% \pm 1$ ps typical
	Accuracy	
	Two-tone	yes
	Adjustable	For each data channel independently, same LFPJ for clock and trigger

Low frequency periodic jitter

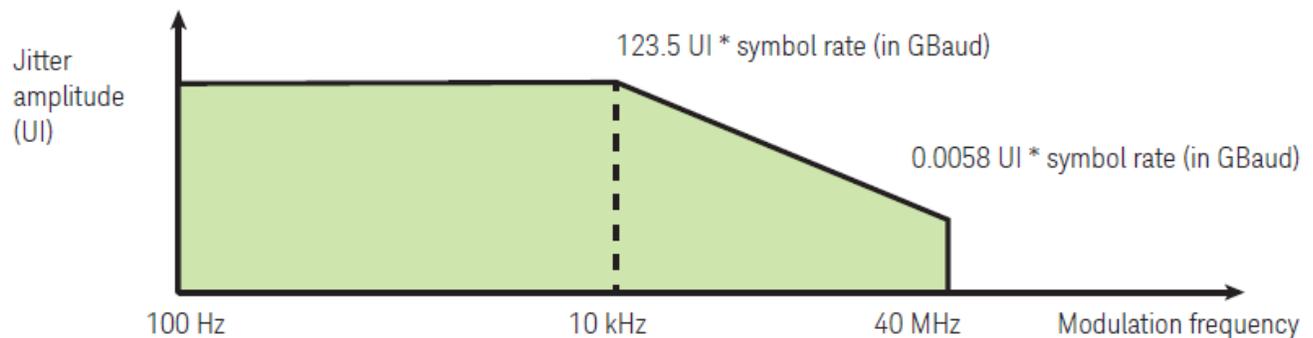


Figure 15. Low frequency periodic jitter maximum depends on data rate and modulation frequency.

**Table 15. Low frequency periodic jitter ranges.**

Symbol rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 10 MHz	Max UI at modulation frequency 40 MHz
2.025 to 4.05 Gbaud	250 to 500 UI	0.0625 to 0.125 UI	0.012 to 0.025 UI
4.05 to 8.1 Gbaud	500 to 1000 UI	0.125 to 0.25 UI	0.024 to 0.048 UI
8.1 to 16.2 Gbaud	1000 to 2000 UI	0.25 to 0.5 UI	0.048 to 0.095 UI
16.2 to 32.4 Gbaud	2000 to 4000 UI	0.5 to 1 UI	0.095 to 0.19 UI
32.4 to 64.8 Gbaud	4000 to 8000 UI	1 to 2 UI	0.19 to 0.38 UI

**Table 16. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter, clock / 2 jitter (all require M8045A Option -0G3 advanced jitter sources)**

High frequency jitter (generated by delay line)	Range	1 UI for > 32.4 Gbaud, for ≤ 32.4 Gbaud minimum of: - 1 UI - 1 UI - (PJ frequency - 250 MHz) / 100 MHz * 0.2 UI - 0.5 UI if RJ low pass filter is 1000 MHz - 0.5 UI if external delay modulation is on Note: This is max sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ.
High frequency periodic jitter (HF PJ1 and HF PJ2)	Range	See HF jitter above <sup>1</sup>
	Frequency	1 kHz to 500 MHz. For symbol rates < 4 Gbaud the max modulation frequency is symbol rate / 8. Two tone possible. Sweep. Sinusoidal
	Jitter amplitude accuracy	±3 ps ± 10% typical <sup>2</sup>
	Adjustable	For each channel independently
Random jitter (RJ)	Range	0 to 72 mUI rms (1 UI p-p max.) <sup>1</sup>
	Jitter amplitude accuracy	±300 fs ± 10% typical
	Filters	High pass: 10 MHz and "off", Low pass: 100 MHz, Low pass: 500 MHz (for symbol rates ≥ 3.75 Gbaud), Low pass: 1 GHz (for symbol rates ≥ 7.5 Gbaud)
	Adjustable	For each channel independently
Spectrally distributed RJ According to PCIe 2 (sRJ) <sup>3</sup>	Range	0 to 72 mUI (1 UI p-p) <sup>1</sup>
	Frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz
	Jitter amplitude accuracy	± 300 fs ± 10% typical
	Adjustable	For each channel independently
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above <sup>1</sup>
	PRBS polynomials	2 <sup>n</sup> -1, n = 7, 8, 9, 10, 11, 15, 23, 31
	Filters	50/100/200 MHz low pass 3rd order
	Jitter amplitude accuracy	± 5 ps ± 10% typical for settings shown in table below
	Adjustable	For each channel independently
	Rate for PRBS generator	625 Mb/s, 1.25 Gb/s, and 2.5 Gb/s
Clock/2 jitter	Range	± 50 mUI or ±5 ps typical (whatever is less). Note: this means that first eye can be up to 50 mUI or 5 ps longer or shorter than subsequent eye
	Adjustable	For each channel independently

1. Range of HF jitter applies to sum of RJ, HF-PJ1 and HF-PJ2, external delay modulation and BUJ. See further limitations under high frequency jitter specifications.
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6 °C
3. Requires M8070B software rev 6.0 or later. sRJ is mutually exclusive with RJ and BUJ. Valid if sRJ low pass filter is "on".

**Table 17. BUJ accuracy applies for these BUJ settings**

BUJ calibration settings <sup>1</sup>	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gb/s	PRBS 2 <sup>9</sup> -1	100 MHz
CEI 11G	2.5 Gb/s	PRBS 2 <sup>11</sup> -1	200 MHz
Gaussian	2.5 Gb/s	PRBS 2 <sup>31</sup> -1	100 MHz
CEI 25G	2.5 Gb/s	PRBS 2 <sup>11</sup> -1	200 MHz
CEI 56G	2.5 Gb/s	PRBS 2 <sup>11</sup> -1	200 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator

**Table 18. specifications for spread spectrum clocking (SSC). Requires M8045A Option -0G3 advanced jitter sources.**

SSC (spread spectrum clock)	Symbol rate range for SSC	2.025 to 32.4 Gbaud
	Range	See HF jitter above <sup>1</sup>
	Asymmetric SSC <sup>1</sup> :	
	Upper deviation range	0 to 1%
	Lower deviation range	-1% to 0
	Frequency	100 Hz to 200 kHz
	SSC amplitude accuracy	± 0.025% typical
Outputs	Can be turned on/ off together for CLK OUT, DATA OUT 1, DATA OUT 2, TRG OUT, Channel 1 and 2 CLK OUT	
Residuals SSC <sup>1</sup>	Range	0 to 600 ps
	Frequency	10 to 100 kHz
	Outputs	Can be turned on/ off together for CLK OUT; DATA OUT 1, DATA OUT 2, TRG OUT, Channel 1 and 2 CLK OUT

1. Requires M8070A SW 5.0 or M8070B SW 6.0 or later.

## External jitter modulation

An external modulation source can be used to modulate the delay of the M8045A data outputs, clock output and trigger output.

## DATA MOD IN 1,2

This input can be used for delay modulation by an external source for each data output channel individually.

**Table 19. Specifications for external jitter modulation on data outputs.**

External jitter – data modulation input 1 and 2	Range	Up to 1 UI for symbol rates > 32.4 Gbaud Up to 0.5 UI for symbol rates ≤ 32.4 Gbaud <sup>1</sup> 0.8 V <sub>pp</sub> max
	Frequency	Up to 500 MHz
Gain	1 UI/ 0.725 V + 5% typical <sup>2</sup>	
Linearity	50 mUI	
Connectors	3.5 mm, female	

1. See HF jitter specifications for the maximum sum of RJ, HF-PJ1 and HF-PJ2 external delay modulation and BUJ
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6°C

## CLK MOD IN

This input can be used for delay modulation of TRIG OUT and CLK OUT, the modulation always affects both outputs.

**Table 20. Specifications for external jitter modulation for clock and trigger.**

External jitter – clock modulation input	Description	Input for the delay modulation for the TRG OUT and CLK OUT. Affects both data outputs
	Range	Up to 1 UI for symbol rates > 32.4 Gbaud Up to 0.5 UI for symbol rates ≤ 32.4 Gbaud <sup>1</sup> 0.8 Vpp max
	Frequency	Up to 500 MHz
Gain		1 UI/ 0.725 V ± 5% typical <sup>2</sup>
Linearity		50 mUI
Connectors		SMA, female

1. See HF jitter specifications for the maximum sum of RJ, HF-PJ1 and HF-PJ2 external delay modulation and BUJ
2. For symbol rates above 32.4 Gbaud at an ambient temperature of 25 ± 6°C

## External Level Interference (RI/SI) Sources

The Keysight M8054A interference source and M8194A, M8195A and M8196A AWG can be used as level interference source with sinusoidal and random modulation. The M8000 system software controls the interference parameters such as amplitude, bandwidth, crest factor. Keysight provides matched coupler pairs for injecting the RI or SI signal before or after the channel. See table below.

**Table 21. Specifications for external level interference sources RI/SI with M8194A, M8195A, M8196A and M8054A.**

	M8070A/B	M8194A	M8195A	M8196A/ M8054A
Random Interference (RI)		Yes	Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	0 mV to 800 mV, 1 mV resolution	0 mV to 1 V, 1 mV resolution	0 mV to 1 V, 1 mV resolution
	Lowest frequency range	230 kHz to 45 GHz	320 kHz -20 GHz (ch1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
	Highest frequency range	230 kHz to 45 GHz	320 kHz to 25 GHz	160 kHz to 32 GHz
	Crest factor (peak ratio)	> 5 <sup>2</sup>	> 5 <sup>2</sup>	> 5 <sup>2</sup>
Sinusoidal interference (SI)		Yes	Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	0 mV to 800 mV, 1 mV resolution	0 mV to 1 V, 1 mV resolution	0 mV to 1 V, 1 mV resolution
	Frequency range	230 kHz to 45 GHz	320 kHz -25 GHz (channel 1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
Common mode sinusoidal interference (CMSI)		Yes	Yes	Yes
	Amplitude	0 mV to 800 mV, 1 mV resolution	0 to 995 mV, 1 mV resolution	0 to 995 mV, 1 mV resolution
	Modulation frequency range	1 MHz to 12 GHz, one and two tone <sup>1</sup>	1 MHz to 12 GHz, one and two tone <sup>1</sup>	1 MHz to 12 GHz, one and two tone <sup>1</sup>
	Phase range	-360 to 360 deg	-360 to 360 deg	-360 to 360 deg
Differential mode sinusoidal interference (DMSI)		yes	Yes	Yes
	Amplitude	0 mV to 800 mV, 1 mV resolution	0 to 995 mV	0 to 995 mV
	Modulation frequency range	1 MHz to 12 GHz, one and two tone <sup>1</sup>	1 MHz to 12 GHz, one and two tone <sup>1</sup>	1 MHz to 12 GHz, one and two tone <sup>1</sup>
	Channel coupling		Yes, for channel 1 & 2, channel 3 & 4	
	Amplitude correction factor <sup>3</sup>	0 to 8.	0 to 10.	
	Phase range	-360 to 360 deg	-360 to 360 deg	-360 to 360 deg
Simultaneous injection of CMSI and DMSI	Simultaneous injection of CMSI and DMSI <sup>1</sup>	0 mV to 800 mV, 1 mV resolution	0 to 995 mV	0 to 995 mV
Recommended accessories	M8045A-802 Matched directional coupler pair, 1 to 50 GHz, 13 dB, 2.4 mm (recommended for RI and highest BW), M8045A-803 Matched coupler pair, DC to 40 GHz, 12 dB, 2.4 mm (recommended for PCIe5, CMSI, DMSI)			
Software pre-requisites	M8070B SW 7.0 or higher	M8194A FW 2.0.31.0 or later and M8070B SW 7.0 or later	M8195A firmware V3.2.0 or higher	M8196A firmware V2.1.0.0 or higher. For M8054A M8070B 6.5 or higher

1. Sum of amplitude in case of two-tone modulation must be within amplitude range

2. Requires M8070B software revision 7.2 or higher

3. Can be used to compensate for differences in channel losses in channel coupling mode

## Emulate ISI (inter-symbol interference) with M8049A

External ISI channel boards are available to emulate channel loss. Keysight M8049A provides 3 different ISI boards with various insertion loss characteristics. M8049A-001 provides 5 short traces, M8049A-002 has 9 medium length traces and M8049A-003 offers 7 long traces.

For detailed specifications see M8049A data sheet.

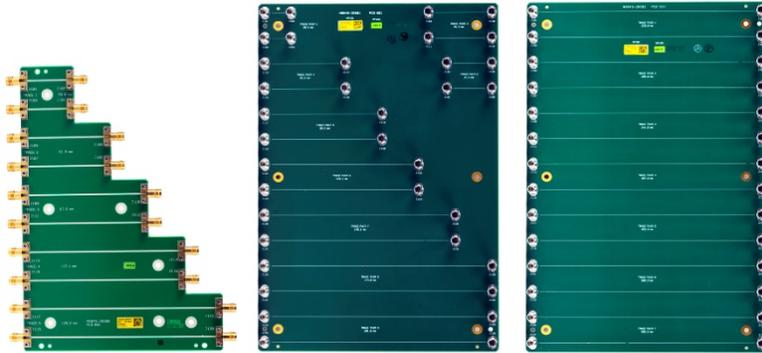


Figure 16. Emulate channel loss for receiver margin testing with Keysight's ISI channel boards

## Pattern Sequencer, Filler Symbol Filtering, and Interactive Link Training

**Table 22. Specifications for pattern, sequencer.**

PRBS <sup>1</sup>	$2n-1$ , $n = 7^2$ , 10, 11, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51, 58
PRBS	$2^n$ , $n = 7, 10, 11, 13, 15, 23$
QPRBS	OIF-CEI: QPRBS13-CEI, QPRBS31-CEI IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q, SSPRQ
PRTS <sup>2</sup>	$3^n-1$ , $n = 7, 17, 19, 23$
New patterns in library	PAM4-linearity, JP03A, JP03B, PAM3-STAIRS64
PAM3 coding <sup>2</sup>	requires M8045A-OP3. Custom symbol mapping
PAM4 coding	Gray coding, custom mapping of 00, 01, 10, 11 to symbols 0, 1, 2, 3. Requires option -OP3 /-OP6.
Mark density	PRBS 1/8 to 7/8
Zero substitution	Yes
Export/Import	Patterns from M8000 and N4900 series can be imported
Pattern library	Yes
User definable memory	NRZ: 2 Gbit/channel, PAM4: 1 G Symbol / channel
Vector/sequence granularity	512 bit
Pattern capture	Yes, raw data for PAM4 <ul style="list-style-type: none"> <li>• Capture data starts on event</li> <li>• User defined (minimum) amount of pre-event bits/ symbols and minimum capture bit/symbols</li> <li>• Events: error, CTRL IN A /B, immediate</li> <li>• Max 2 Gbit/ch capture data for NRZ, 1 G Symbol / ch for PAM4</li> </ul> Save captured data: <ul style="list-style-type: none"> <li>• With errors</li> <li>• As expected, data (ignores error content)</li> <li>• As PG data (ignores error content)</li> <li>• Export via pattern editor windows</li> <li>• Convert bits into all other codings and vice versa</li> <li>• Ability to mask error bits automatically</li> </ul> Display of captured data: <ul style="list-style-type: none"> <li>• Display errors with color coding</li> </ul> Navigate through error bits/symbols (find next/previous)
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.

1. Polarity is inverted compared to ParBERT and J-BERT N4903A/B and N49xx series.

2. M8045A only

## Filtering of SKPs, SKP OS and ALIGNs (M8046A Option -0S2, Option -0S4, -0S6, -0N2)

SKPs, SKP OS and ALIGN are filler symbols used for clock compensation. Filtering of such symbols is required whenever a device under test (DUT) modifies respective filler symbols embedded in the test pattern. This is always the case when the DUT and BERT are operated with independent clocks but dependent on the loopback implementation in the DUT it can happen with synchronized clocks as well. Whenever SKP OS or ALIGN filtering is enabled, it is required to use a test pattern version including SKP OS or ALIGNs in the pattern generator sequence and an expected test pattern version without SKP OS or ALIGNs in the error detector sequence. Respective patterns are part of the factory pattern library. This functionality requires M8046A-0S2 for PCIe, M8046A-0N2 for PCIe at 64 GT/s, M8046A-0S4 for USB 3.2, or M8046A-0S6 for SATA/SAS and a M8070B software revision 6.0 or later.

**Table 23. Specifications for SKP OS and ALIGN filtering (M8046A Option -0S2, -0S4, -0S6)**

Standard		Software revision and license needed
PCIe	64 GT/s with 1b/1b coding	Requires M8046A-0N2, -0S2 and M8070B SW rev 8.0 or later
	8/ 16/ 32 GT/s with 128b/ 130b coding	Requires M8046A-0S2 and M8070B SW rev 6.5 or later
	5 GT/s with 8b/ 10b coding	Requires M8046A-0S2 and M8070B SW rev 6.7 or later
	2.5 GT/s with 8b/ 10b coding	Requires M8046A-0S2 and M8070B SW rev 7.0 or later
CCIX	20 / 25 GT/s	Requires M8046A-0S2 and M8070B SW rev 6.5 or later
USB	5 Gb/s with 8b/ 10b coding	Requires M8046A-0S4 and M8070B SW rev 6.7 or later
	10 Gb/s with 128b/ 132b coding	
SATA/SAS	3 / 6 Gb/s with 8b/ 10b coding	Requires M8046A-0S6 and M8070B SW rev 6.7 or later
	12 Gb/s with 8b/ 10b coding	

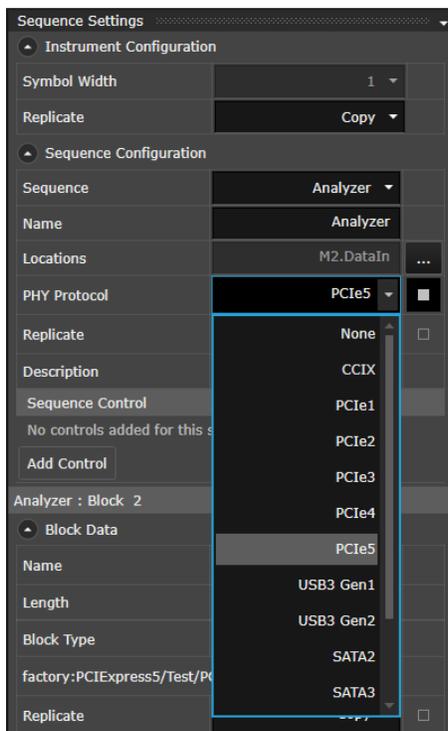


Figure 17. Users can select in the pattern sequencer menu between PCIe6, PCIe5, PCIe4, PCIe3, PCIe2, PCIe1, SAS 3, SAS 2, SAS 1, SATA 3, SATA 2, CCIX, USB 3.0 (5 Gb/s) or USB 3.1 (10 Gb/s) as PHY protocol to enable to the SKP OS and ALIGN filtering feature with M8046A-0S2/-0N2 (PCIe), -0S4 (USB), or -0S6 (SATA/SAS)

## Interactive Link Training for PCIe

In some industry standards, such as PCIe, the transmitter de-emphasis and receive equalization must be optimized during a training sequence to compensate for the actual channel loss caused by PC board materials.

For testing receivers of such interfaces, you need an error analyzer that understands the low-level protocol of the bring-up sequence including speed changes and triggering changes of the pattern generator's de-emphasis setting.

M8046A provides a link training status state machine that supports PCIe 8, 16, and 32 GT/s. It is suitable to test the root complex and end point. Supports 2 channels.

Pre-requisites for this functionality:

- Module hardware: M8046A Option -0S1. Requires M8045A and M8046A modules with a high-speed communication link (LINK 1234), which are available for all serial numbers of MY/DExxx01000 or later. The M8046A-0A4 integrated clock recovery and a pattern generator with M8045A-0G4 de-emphasis is also required. M8046A-0S2 is recommended.
- Software: M8070B rev 6.7 or later.

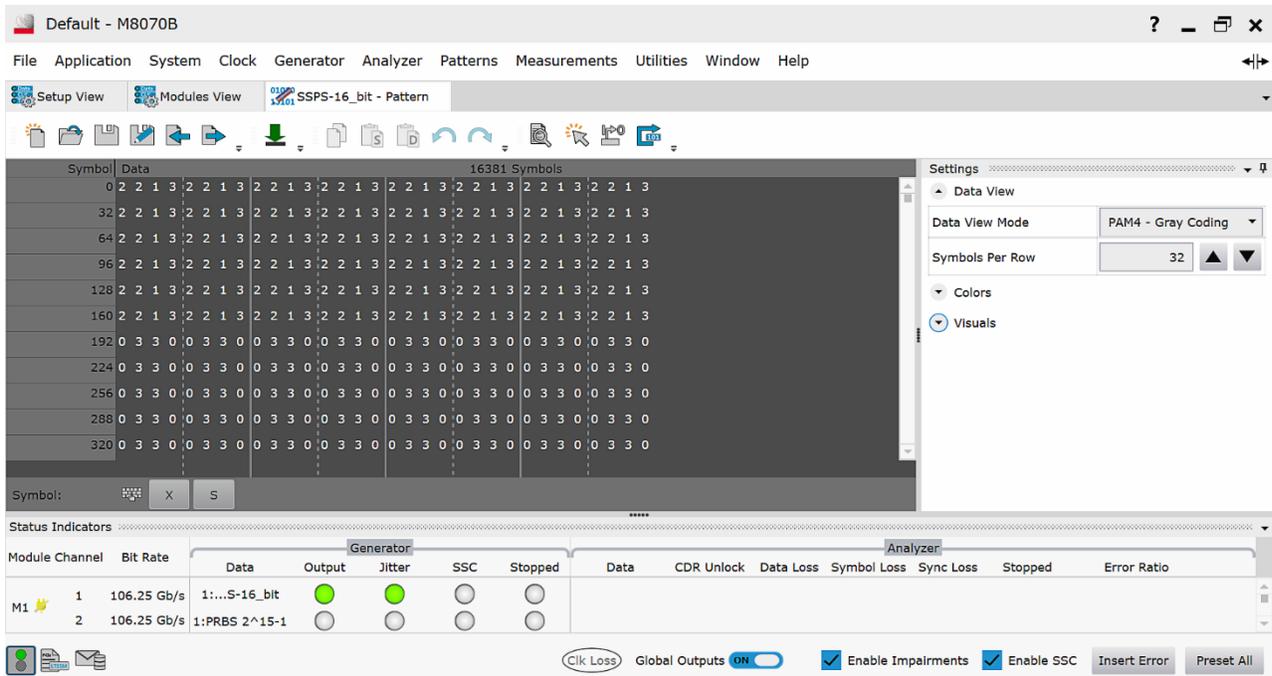


Figure 18. The pattern editor in the M8070B software allows editing NRZ bits and PAM4 symbols. The PAM4 symbol to bit mapping can be selected as Gray coded or custom with adjustable PAM4 levels. Quaternary PRBS, like QPRBS13-CEI or QPRBS31, according to CEI and IEEE standards can be selected as well as SSPRQ and PAM4 linearity test patterns.

## Interactive Link Training for USB 3.2

USB 3.2 compliance testing requires the product under test to enter loopback, a state at which the product under test sends the incoming bitstream at its receiver back from its transmitter without applying error correction. In order to enter loopback, the product under test must go through several LTSSM (Link Training Status State Machine) handshakes during which the link speed and bandwidth are negotiated, as well as the receiver equalization fine-tuned.

M8046A provides a USB 3.2 interactive LTSSM that adapts to the timing requirements of the product under test, making the link training step trivial, helping you focus on the actual receiver test.

Furthermore, the USB 3.2 specification defines dual-lane (x2) mode for the USB Type-C connector. In this mode, both transmitters and receivers operate simultaneously, producing aggregate bit rates of 10 Gb/s (5 Gb/s x2) and 20 Gb/s (10 Gb/s x2). A product that can operate in x2 mode must be tested accordingly, as close as possible to operating conditions. To do so, the M8040A High-Performance BERT allows the usage of a second M8046A module to enable interactive link training functionality for both lanes concurrently.

Pre-requisites for this functionality:

- Module hardware: M8046A Option -0S3. Requires M8045A and M8046A modules with a high-speed communication link (LINK 1234), which are available for all serial numbers of MY/DExxx01000 or later. The M8046A-0A4 integrated clock recovery is also required. M8046A-0S4 is recommended.
- If testing dual lane mode: a second M8046A module with same configuration and an M8045A module with two licensed channels.
- Software: M8070B rev 7.5 or later.

## Specifications Analyzer Module (Error Detector) M8046A



Figure 19. Front panel of M8046A

The M8046A supports symbol rates up to 32 Gbaud and 64 Gbaud, the default is 32 Gbaud and NRZ format. The analyzer module can be used for error analysis in conjunction with the M8045A pattern generator and the M8195A/M8196A arbitrary waveform generator. For the following functions a separate module option is required:

- PAM4 decoding up to 32 Gbaud (M8046A Option -0P3), extension to 58 Gbaud (M8046A Option -0P6)
- Equalization for symbol rates above 32.4 Gbaud (M8046A Option -0A3)
- Analyzer, 1 channel, data rate up to 64 Gbaud, NRZ (M8046A Option -A64)
- Clock recovery up to 32 Gbaud (M8046A Option -0A4), extension to 64 Gbaud (M8046A Option -0A5)
- Interactive link training for PCIe 8/ 16/ 32 GT/s (M8046A Option -0S1)
- Interactive link training for USB 3.2, 5/ 10 Gb/s, x1/ x2 (M8046A Option -0S3)
- SKP OS filtering for PCIe 2.5<sup>1)</sup>/ 5/ 8/ 16/ 32/ 64 GT/s and CCIX 20/25 Gb/s (M8046A Option -0S2)
- SKP OS filtering for USB 3.0, 3.1, 3.2 (M8046A Option -0S4)
- ALIGN filtering for SATA 3<sup>1)</sup>/6 Gb/s and SAS 3<sup>1)</sup>/6/12 Gb/s (M8046A Option -0S6)

<sup>1</sup> requires integrated clock recovery M8046A Option -0A4/-0A5

## Data input (DATA IN)

**Table 24. Data input characteristics for M8046A.**

Symbol rate <sup>7</sup>	2.45 to 32.4 Gbaud NRZ for M8046A-A32, 2.45 to 32.4 Gbaud PAM4 for M8046A-A32 with -0P3 For modules with a serial number below MYxxx02000 the range is 5.0 to 30.0 Gbaud 2.45.0 to 64.8 Gbaud NRZ for M8046A-A64 2.45.0 to 58 Gbaud PAM4 for M8046A-A64 with -0P3, -0P6 and -0A3 (all specifications are valid up to 53.2 Gbaud with over-programming). Requires serial number above MYxxx02000.
Channels per module	1
Data format	NRZ (default) PAM4 (requires M8046A Option -0P3 and for symbol rates above 32.4 Gbaud M8046A Option -A64, --0P3, -0P6, -0A3)
Max # of M8046A per M9505A chassis	up to 4
Input sensitivity <sup>1,3,7</sup>	For symbol rates from 2.45 to 32.4 Gbaud for NRZ and PAM4: 12% of input range setting + 30 mV eye height per eye, single ended and differential. For BER of 10 <sup>-12</sup> . <b>NRZ:</b> 32.5 to 64.2 Gb/s: 16% of input range setting + 35 mV eye height single ended and differential. For BER of 10 <sup>-12</sup> <b>PAM4:</b> 32.5 to 53.2 Gbaud <sup>2</sup> : 12% of input range setting + 15 mV eye height per eye, single ended and differential. For BER of 10 <sup>-6</sup> For modules with a serial number below DExxx00515 these specifications apply: NRZ: 70 mV single ended and differential PAM4: 70 mV per eye single ended and differential
Max input voltage amplitude	1600 mV pp differential for balanced patterns. For modules with serial number below DExxx00515: <b>1000 mVpp differential</b>
Input voltage window	-1 V to +3 V
Termination voltage <sup>5</sup>	-1 V to +3 V for modules with serial number above DExxx00515
Timing resolution	0.1 ps
Input bandwidth (3dB)	16 GHz with smooth roll-off
Sampling point	Manual <sup>6</sup> and automatic. Finds optimum voltage range, threshold and delay of the sampling point. Delay accuracy is 20 mUI or 1.5 ps whichever is higher. <sup>4</sup> One sampling edge per UI.
Decision threshold range	Full input voltage range with 1 mV resolution

Equalizer modes

- Automatic equalizer coefficient optimization
- Equalizer presets with standard analyzer data input cable compensation. The equalizer gain is controlled as equalizer level, and the losses of the standard cabling is automatically included in the equalizer setting
- Manual coefficient entry with cable compensation. The coefficients of the FFE (Feed Forward Equalizer) can be entered manually. Additionally, the losses of the standard cabling are automatically included in the equalizer setting
- Manual coefficient entry. The coefficients of the FFE can be entered manually. No cable losses are automatically compensated. Use this mode when using non-standard cabling.

Automatic equalizer coefficient optimization

Requires an input signal with random-like pattern. It's an iterative procedure to minimize BER. This function requires M8070B software rev 6.0.210 or later. This table shows the maximum loss<sup>9</sup> that can be compensated for symbol rates above 32 Gbaud:

Symbol rate	NRZ		PAM4	
	With external clock <sup>9</sup>	With CR	With external clock <sup>9</sup>	With CR
32 Gbaud	18.5 dB	16.5 dB	11.0 dB	9.0 dB
35 Gbaud	18.0 dB	16.0 dB	10.0 dB	8.5 dB
40 Gbaud	16.0 dB	16.0 dB	9.5 dB	8.5 dB
45 Gbaud	15.0 dB	13.0 dB	8.5 dB	8.5 dB
50 Gbaud	14.5 dB	12.5 dB	7.5 dB	5.0 dB
53.125 Gbaud	14.0 dB	12.0 dB	5.0 dB	1.5 dB
56 Gbaud	13.5 dB	12.0 dB	1.5 dB	0 dB
58 Gbaud	13.0 dB	12.0 dB	0 dB	0 dB

External redriver

For higher channel loss compensation, e.g. for testing PCIe server boards, the M8047A can be used together with M8046A. M8047A can be controlled from M8070B. See M8047A datasheet for more details.

Equalizer presets with cable compensation

For symbol rates up to 32 Gbaud:  
 Up to 13 dB at 32.4 Gbaud NRZ.  
 Up to 5.5 dB at 29 Gbaud PAM4.  
 Up to 5.1 dB at 26.5625 Gbaud PAM4  
 FFE with 55 presets for PAM4 and 120 presets for NRZ. See figure below.  
 No Equalizer license is needed below 32 Gbaud.

For symbol rates above 32 Gbaud: the use of presets is not recommended. Please use automatic equalize tap optimization to achieve the best results:  
 Up to 3 dB at 58 Gb/s for NRZ signals.  
 (requires M8046A-0A3 and -A64): 120 presets for NRZ, FFE.

Manual equalizer coefficients

16 (FIR) filter coefficients, numbered from 0 to 15.  
 Coefficient 2 is the main-cursor and cannot be changed. The available value range is:

- Coefficient 0: -0.25 to + 0.25
- Coefficient 1: -0.5 to + 0.5
- Coefficient 2: 1.0
- Coefficient 3: -0.5 to +0.5
- Coefficient 4: -0.25 to + 0.25
- Coefficient 5: -0.125 to +0.125
- Coefficient 6 to 15: -0.0625 to +0.062

The sum of all 16 coefficients may not be 0

Phase margin NRZ	1 UI – 12 ps typical for PRBS 2 <sup>15</sup> – 1 @ BER of 10 <sup>-12</sup>
Phase margin PAM4	1 UI – 8 ps typical for clock pattern @ BER of 10 <sup>-12</sup> 280 mUI typical, measured at 26.5625 Gbaud with PRBS 2 <sup>15</sup> -1 @ BER of 10 <sup>-12</sup> 200 mUI typical, measured at 32.4 Gbaud with PRBS 2 <sup>15</sup> -1 @ BER of 10 <sup>-12</sup> 100 mUI typical, measured at 53.2 Gbaud with PRBS 2 <sup>15</sup> -1 @ BER of 10 <sup>-6</sup>
Interface	Differential: 100 Ω nominal, Single ended: 50 Ω nominal DC coupled, terminate unused input with 50 Ω For modules with a serial number below DExxx00515: AC coupled, terminate unused input with 50 Ω
Connectors	2.4 mm, female

1. Measured with PRBS 2<sup>15</sup> – 1
2. Measured between 100 and 400 mV input range and with a module serial number MYxxx02000 and higher
3. Valid at room temperature.
4. With 48 to 52% duty cycle at CLK IN signal.
5. Termination voltage must be within a window of DC common mode voltage ± 1.5 V.
6. For symbol rates < 4.9 Gbaud the automatic alignment is recommended after recovery from clock loss
7. For serial numbers below MYxxxx2100 the minimum symbol rate is 5 Gbaud, CDR mode only.
8. Measured with M8049A-002 and M8049A-003 and automatic equalization optimization
9. Measured with a clean clock from M8045A channel clock output

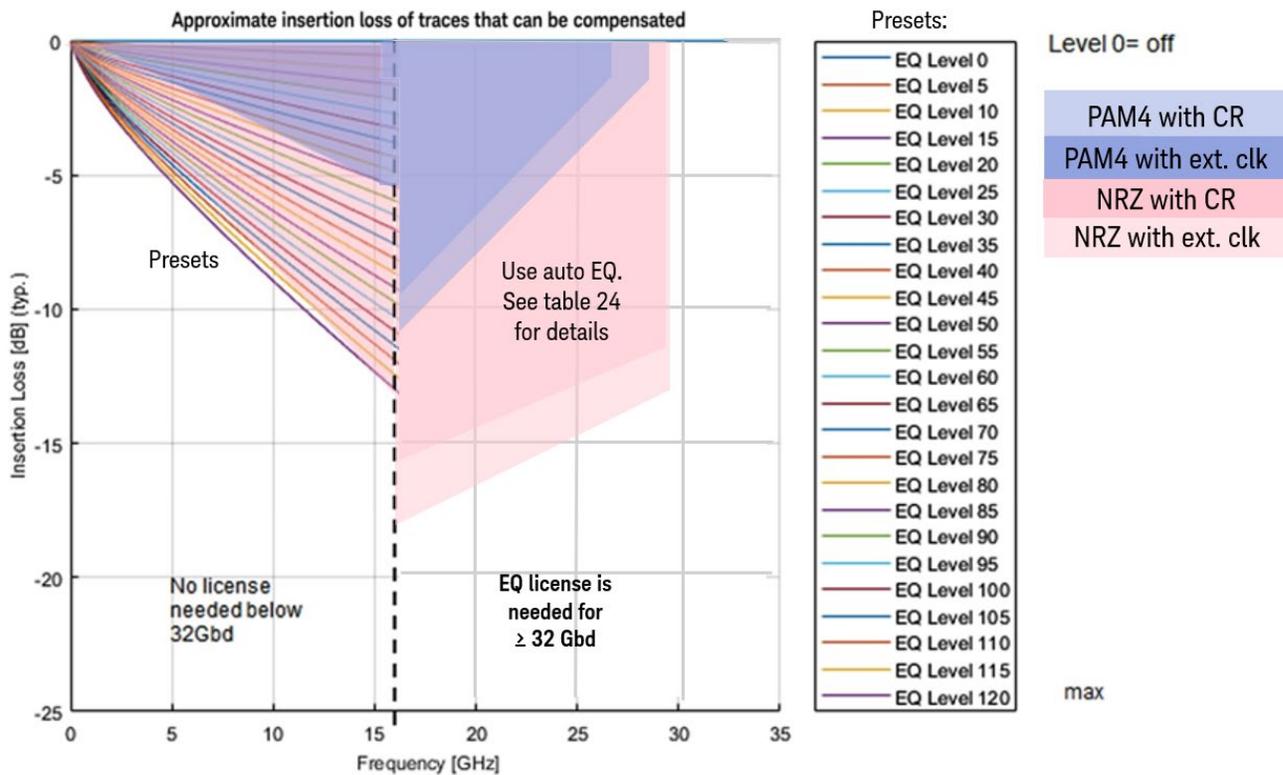


Figure 20. The M8046A provides built-in equalization to reduce channel loss in the loop back channel. The available ranges for PAM4 and NRZ signals up to 64 Gbaud are shown here. For symbol rates above 32 Gbd the M8046A-0A3 equalizer option is required.

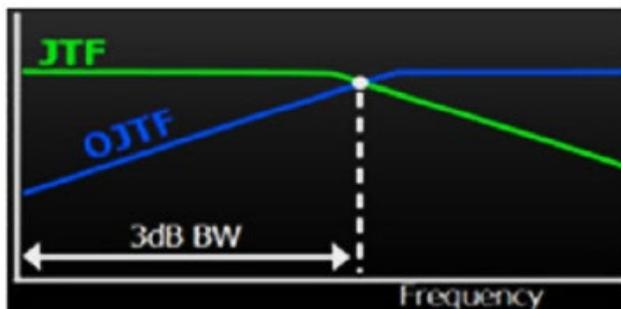
**Table 25. Specifications for integrated clock recovery (requires M8046A option 0A4, 0A5).**

	Comment	M8046A Option 0A4/UA4 and 0A5/UA5
CR symbol rate range <sup>2</sup>		NRZ: 2.45 to 32.4 Gb/s (requires M8046A option -0A4) NRZ: 2.45 to 64.8 Gb/s (requires M8046A options -A64, -0A4 and -0A5) PAM4: 2.45 to 32.4 Gbaud (requires M8046A with options -0A4 and -0P3) PAM4: 2.45 to 58 Gbaud (all specifications are valid up to 53.2 Gbaud with over-programming), (requires M8046A options -A64, -0A4, -0A5, -0P3, -0P6, and -0A3)
Selectable loop type	First and second order PLL - see figure below for description	Yes
Tunable loop bandwidth <sup>3</sup>		2 to 20 MHz. For second order PLL the range depends on selected peaking. 4 to 16 MHz with PAM4 and symbol rate > 32.4 Gbaud <sup>1</sup>
Loop bandwidth accuracy		± 30% typical for symbol rates ≥ 4.9 Gbaud
Transition density		25-100%
Clock recovery peaking range		Up to 4 selectable settings (dependent on loop bandwidth and baud rate)
Acquisition	Input symbol rate must be within the range of ± 500 ppm of the set symbol rate	± 500 ppm typical
Tracking range	SSC can be tracked when symbol rate is set to center frequency. SSC frequency ≥ 30 kHz	± 3000 ppm typical (for symbol rate up to 32.4 Gbaud)
CDR freeze		Not provided

1. There is no limitation to set the loop bandwidth in the range of 2 to 20 MHz, but it may not lock.
2. For SN below 2100 minimum symbol rate is 5 Gbaud, below SN 2100 min symbol rate is 5 Gbaud.
3. Below 4.05 Gbaud maximum loop bandwidth is 10 MHz

### First order PLL (type 1)

- A type 1 is defined by bandwidth. No peaking.
- JTF bandwidth = OJTF bandwidth.
- Used by some communication standards



### Second order PLL (type 2)

- A type 2 is defined by JTF loop bandwidth. No peaking.
- JTF bandwidth > OJTF bandwidth.  
Used by some computing standards

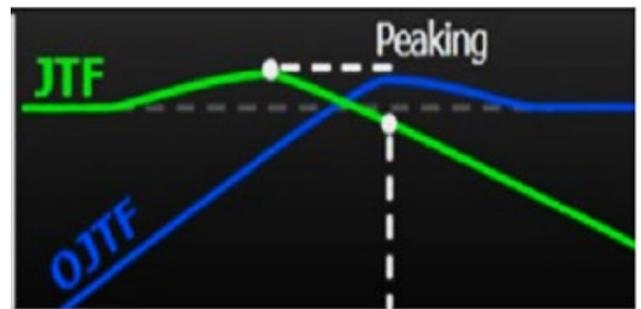


Figure 21. The M8040A provides a built-in- clock recovery option. You can choose between a first and second order PLL characteristic

## External clock input (CLK IN)

**Table 26. specifications for clock input of analyzer**

Amplitude	Minimum 200 mVpp, maximum 1 Vpp
Frequency range <sup>1</sup>	2.5 to 32.4 GHz Note: In clk "x 2" mode for symbol rates above 25 Gbaud an external bandpass filter (M8061A-803) has to be used on the clock input. The filter has to be removed for symbol rates below 25 Gbaud. In clk "x 1" mode no filter is needed.
Multiplier internal	1,2
Connector	3.5 mm, female

1. Below 5 GHz transition time of clock signal should be < 25 ps

## Recovered clock output (REC CLK OUT)

This output provides a recovered clock when using the integrated clock recovery function of M8046A. It can be used to trigger a DCA sampling oscilloscope. It is only provided for M8046A modules with S/N above DExxx1000.

**Table 27. Specifications for recovered clock output of analyzer.**

Amplitude	Fixed 600 mVpp typical
Symbol rate	Symbol rate at data inputs/2 (maximum of 16.2 GHz)
4.9 to 32.4 Gbaud	
Symbol rate $\geq$ 32.4 Gbaud	Symbol rate at data inputs/4 (maximum of 16.2 GHz)
Connector	3.5 mm, female

## SYNC input (SYNC IN)

Can be used to clock the analyzer from the pattern generator's M8045A system clock via the sync output A/B (requires cable M8051A-801). Not needed if external clock is used. This input is only available for M8046A modules with a serial number below DExxx01000.

## Control input A (CRTL IN A)

Functionality can be selected as: sequence trigger, pattern capture event

**Table 28. Specifications for control inputs of analyzer.**

Input voltage	-1 to -3 V
Termination voltage	-1 to -3 V
Termination voltage accuracy	$\pm$ (25 mV +1%)
Threshold voltage	-1 to -3 V
Response time	$\pm$ 512 UI repeatability
Connector	3.5 mm, female

## Control output (CTRL OUT A)

Outputs a pulse in case of an error. Generates a pulse or static high/low if used from sequencer.

**Table 29. control output specifications for M8046A.**

Amplitude	0.1 to 2 V
Output voltage	- 0.5 to 1.75 V
Delay from data input	< 1 ms, repeatability $\pm 512$ UI (requires M8070A software 4.5/ M8070B 6.0 or later)
Connector	3.5 mm, female

## Communication link (LINK 1234)

This communication link provides a low latency communication path between M8045A and M8046A modules for enabling interactive link training, e.g. For 5/ 8/ 16/ 32Gb/s PCIe. It requires the cable M8051A-801. This interface is available for M8046A modules with a serial number above DExxx01000. Upgrades are available for older serial numbers (M8046A-US1, requires return-to-Keysight).

## Measurements

**Table 30. Measurement capabilities.**

		M8070A	M8070B	M8070ADVB	M8070EDAB
BER, SER	Accumulation and instantaneous	Yes	Yes		
Jitter tolerance		Yes	No	Yes	
BERT Scan with RJ, DJ separation		No <sup>2</sup>	No	No <sup>2</sup>	
Output level and Q-factor		No	No	No	
Sampling point view		Yes <sup>1</sup>	Yes		
Counters	Compared bits, errored bits Compared 0 bits, errored 0 bits Compared 1 bits, errored 1 bits Compared symbols, errored symbols Compared symbols 0, 1, 2, 3 Errored symbols 0, 1, 2, 3	Yes	Yes		
BER versus parameter automated sweep		Yes	No	Yes	
Error distribution analysis		No	No	No	Yes

1. Requires M8070A SW 4.0/M8070B SW 6.0 or later.

2. The measurement is available in the user interface, but just for debugging/troubleshooting purposes. The accuracy of jitter separation results is unspecified in case of NRZ and invalid in case of PAM4 signals.

## External clock recovery

The Keysight N1076A/B, N1077A, N1078A electrical and optical clock recovery units can be used to recover a clock from NRZ and PAM4 patterns to clock the M8046A error analyzer. The clock recovery units can be controlled from the M8000 system software for BER and jitter tolerance testing.

**Table 31. Conditions for use of external clock recovery.**

	N1076A/77A	N1076B/78A	
Symbol rate	PAM4: 0.05 to 32.8 Gbaud (characteristic) <sup>1</sup>	PAM4: 0.125 to 65.6 Gbaud (characteristic) <sup>1</sup>	
Sensitivity with recommended accessories	30% of input range + 45 mV for M8046A with serial number above DExxx00515 (single ended and differential). For M8046A modules with a serial number below DExxx00515 these specifications apply: NRZ: 200 mV PAM4: 120 mV per eye		
Number of consecutive symbols without transition	NRZ: 144 PAM4: 72 (144 bit)		
Measurements	Jitter tolerance, BER		
Software pre-requisites	M8070A 3.6 or higher N1010A Flex DCA A.05.61 or higher, no extra licenses needed	M8070B 6.0 or later and M8070ADV B N1010A Flex DCA A.05.80 or higher, no extra licenses needed	
	Note: The M8070A/B and the N1010A controlling the external clock recovery units should run on the same controller. The N1010A Flex DCA software cannot be operated interactively while being controlled by M8070A/B. If a DCA-M is used in the same test setup, we recommend to controlling it from a second PC/ controller.		
Hardware pre-requisites	N1076A-232 or N1077A-232 for symbol rates above 16 Gbaud M8046A-A32 with serial number above DE xxx00200.	For symbol rates above 32 Gbaud: N1076B-264/N1078A-264 and M8046A-A64	
Recommended accessories (for differential signals)	<ul style="list-style-type: none"> <li>Qty 1 of Keysight N1027A-2P2 microwave pick-off tee, 2.4 mm connectors, matched pair</li> <li>Qty 2 of Keysight 11900B adapter 2.4mm (f) to 2.4mm (f)</li> </ul>	For rates above 32 Gbaud: <ul style="list-style-type: none"> <li>Qty 1 of Keysight N1027A-2P1 microwave pick-off tee, 1.0 mm connectors, matched pair</li> <li>Qty 2 of Keysight 11921B adapter 1mm (m) to 1.85mm (f)</li> <li>Qty 2 of Keysight 11921F Adapter 1.85mm (f) to 1.0 mm (f)</li> </ul>	For rates below 30 Gbaud: <ul style="list-style-type: none"> <li>Qty 1 of Keysight N1027A-2P8 microwave pick-off tee, 1.85 mm connectors, matched pair</li> <li>Qty 2 of Keysight 11900B adapter 2.4mm (f) to 2.4mm (f)</li> </ul>
	<ul style="list-style-type: none"> <li>Qty 2 of Keysight 83059A adapter 3.5 mm (m) to 3.5mm (m) for mounting the pick-off tee directly to inputs of N107xA/B</li> <li>Qty 1 of Keysight M8046A-802 matched cable pair 2.4 mm, 2 ps</li> </ul>		

<sup>1</sup> range depends on selected option.

## Error Analysis of PAM4 Signals Using an UXR-Series

Error analysis of PAM4 signals is analyzed using the M8046A error detector. For analyzing the errors of PAM4 signals with symbol rates above 30 Gbaud, the M8000 system software rev 4.0 or higher supports the use of a Keysight real-time oscilloscope for capturing the signal and decoding it into a pattern stream. The M8000 system software can upload the acquired pattern and handle the synchronization and comparison with an expected pattern even for long PRBS polynomials such as PRBS31Q. This method allows measuring target BERs up to of  $10^{-6}$  for symbol rates up to 64 Gbaud within reasonable measurement times (~ 1minute) and using the adjustable equalization and clock recovery functions of the oscilloscope. See table below for more details.

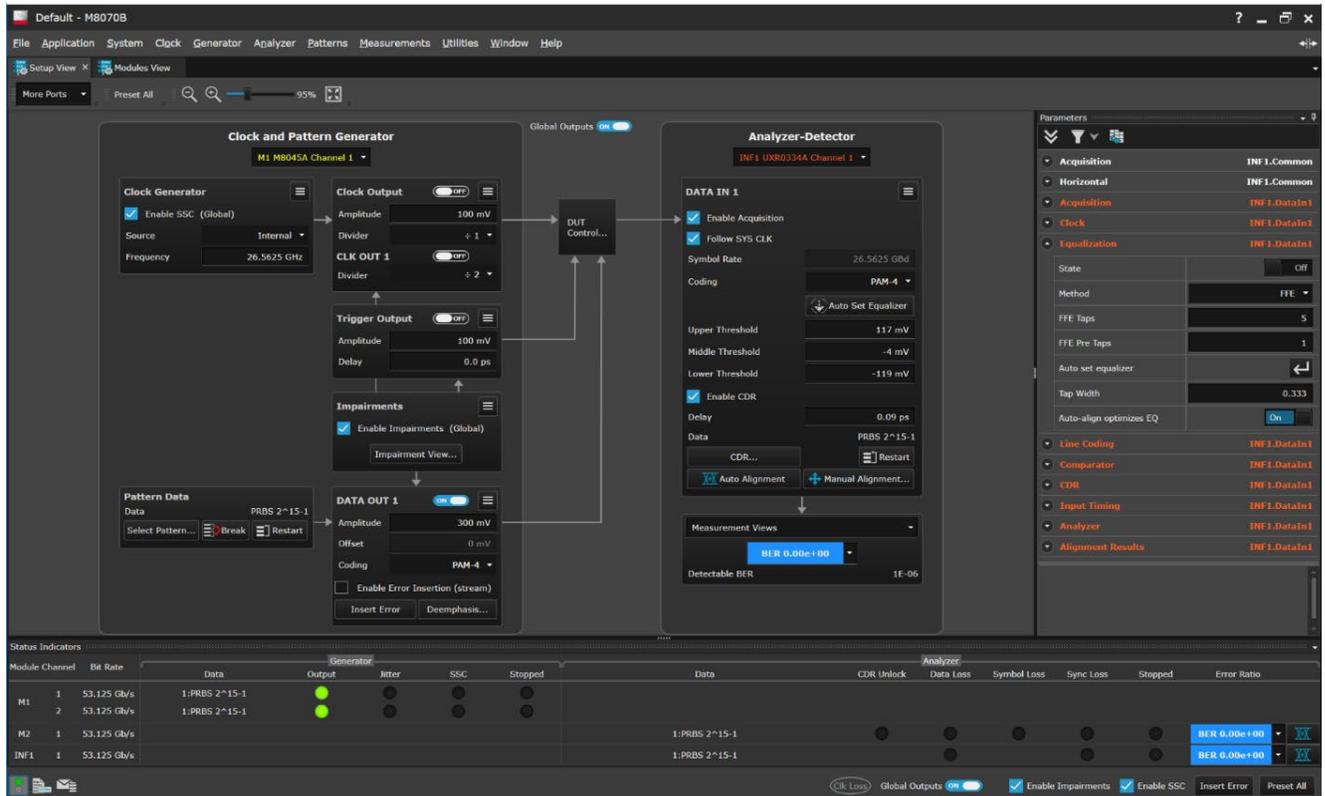


Figure 22. The setup view of the M8070B system software displays all major BERT pattern generator and error analyzer parameters at a glance. The example shows the Analyzer-Detector is using the Keysight UXR0334A real-time oscilloscope for error analysis of a 53 Gbaud PAM4 signal. At the right you can adjust the acquisition, equalizer, clock recovery parameters of the connected DSAZ634A or UXR.

**Table 32. Conditions for error analysis with M8070ADVB using a real-time oscilloscope for symbol acquisition.**

Symbol rates	14 to 58 Gbaud PAM4 for DSAZ634A with real edge inputs. 14 to 110 Gbaud PAM4 for UXR1104A
Target BER	10 <sup>-6</sup>
Coding	PAM4, NRZ
Expected patterns	User definable: PRBS 2n-1 with n = 7, 9, 10, 11, 13, 15, 23, 31, 33, 35, 39, 41, 45, 47, 49, 51 Memory patterns with max. pattern length of 256 kbit
Measurements	Jitter tolerance, BER and SER
Measurement time	Depends on: <ul style="list-style-type: none"> <li>• Expected pattern type</li> <li>• Expected pattern length (in case of memory patterns)</li> <li>• Symbol rate</li> <li>• Equalizer usage and parameters</li> <li>• Acquisition depth in UI</li> <li>• Target BER and confidence level</li> </ul>
BER and symbol counters	BER counters <ul style="list-style-type: none"> <li>• Compared bits</li> <li>• Errored bits</li> <li>• Compared 0 bits, compared 1 bits</li> <li>• Errored 0 bits, errored 1 bits</li> </ul> Symbol counters: <ul style="list-style-type: none"> <li>• Compared symbols</li> <li>• Errored symbols</li> </ul> For each symbol level: <ul style="list-style-type: none"> <li>• Compared symbols</li> <li>• Errored symbols</li> </ul>
Parameters	Acquisition Number of bits per acquisition. (Note: The maximum number of bits per acquisition is limited by the oscilloscope's acquisition memory depth, symbol rate and clock recovery setting.) <ul style="list-style-type: none"> <li>• Global acquisition bandwidth limit</li> <li>• Channel bandwidth limit and filter type</li> <li>• Pattern capture up to 100 Mbit</li> </ul> Horizontal reference clock: internal, external 10 MHz and 100 MHz Clock: Follow Sys Clock, symbol rate Line Coding <ul style="list-style-type: none"> <li>• Coding (NRZ / PAM4)</li> <li>• Symbol mapping (uncoded, Gray, custom)</li> <li>• Custom symbol mapping</li> </ul> Comparator <ul style="list-style-type: none"> <li>• Compare mode (single ended / differential)</li> <li>• Polarity (non-inverted / inverted)</li> <li>• Auto-set thresholds</li> <li>• User-defined thresholds</li> </ul> Equalizer FFE- Number of taps <ul style="list-style-type: none"> <li>• FFE- Number of pre-taps</li> <li>• FFE - Auto-set coefficients</li> <li>• CTLE - DC gain</li> <li>• CTLE - Frequency pole #1, Frequency pole #2,</li> <li>• CTLE - Frequency zero #1</li> <li>• DFE- Taps</li> <li>• DFE-Auto-set coefficients</li> </ul> Clock Recovery (2nd Order CR) <ul style="list-style-type: none"> <li>• Loop bandwidth</li> <li>• Symbol rate divider</li> </ul>

	<ul style="list-style-type: none"> <li>• Damping factor</li> <li>• Sample delay (PAM4 only)</li> <li>• Auto alignment</li> <li>• Covers thresholds, sample delay and equalizer coefficients</li> </ul> Automatically set scope parameters <ul style="list-style-type: none"> <li>• Thresholds</li> <li>• FFE coefficients (cannot be changed by user)</li> <li>• Sample delay position (in case of NRZ)</li> </ul>										
Supported real-time oscilloscope models	<ul style="list-style-type: none"> <li>• Keysight UXR series, all models from 33 to 110 GHz ( 2 or 4 channels)</li> <li>• Keysight DS0Z634A, DSAZ5634A</li> <li>• Keysight DSOC96204Q, DSAX96204Q</li> <li>• Keysight DSAZ594A*, DSOZ594A*</li> <li>• Keysight N7005A 60 GHz Optical-to-Electrical Converter ( requires M8070B SW 8.0 or later and Infiniium UXR with AutoProbe III interface (≥ 40 GHz))</li> <li>• Note: Z-Series Oscilloscope needs real-edge inputs, Models with bandwidth &lt;64 GHz impact the maximum symbol rate</li> <li>• *require M8070A SW version 4.5 or higher</li> </ul>										
Software pre-requisites	<table border="1"> <tr> <td>DSO/DSA (Z-series)</td> <td>UXR</td> </tr> <tr> <td>M8070A SW version 4.5 or higher</td> <td>M8070B system software for M8000: version 6.5 or higher and M8070ADVB</td> </tr> <tr> <td>Minimum supported Infiniium version is 06.10.00616</td> <td>Minimum supported Infiniium version is 10.10</td> </tr> <tr> <td>Following licenses are required on the oscilloscope in addition:</td> <td>Following licenses are required on the oscilloscope in addition:</td> </tr> <tr> <td> <ul style="list-style-type: none"> <li>• N5384A Serial Data Analysis (SDA)</li> <li>• N8827A PAM4 measurement (PM4)</li> <li>• N5461A Equalization (DEQ)</li> </ul> </td> <td> <ul style="list-style-type: none"> <li>• D9010PAMA Pulse Amplitude Modulation PAM-N analysis Software</li> <li>• D9020ASIA Advanced Signal Integrity software (EQ, InfiniSim, Adv, Crosstalk)</li> </ul> </td> </tr> </table>	DSO/DSA (Z-series)	UXR	M8070A SW version 4.5 or higher	M8070B system software for M8000: version 6.5 or higher and M8070ADVB	Minimum supported Infiniium version is 06.10.00616	Minimum supported Infiniium version is 10.10	Following licenses are required on the oscilloscope in addition:	Following licenses are required on the oscilloscope in addition:	<ul style="list-style-type: none"> <li>• N5384A Serial Data Analysis (SDA)</li> <li>• N8827A PAM4 measurement (PM4)</li> <li>• N5461A Equalization (DEQ)</li> </ul>	<ul style="list-style-type: none"> <li>• D9010PAMA Pulse Amplitude Modulation PAM-N analysis Software</li> <li>• D9020ASIA Advanced Signal Integrity software (EQ, InfiniSim, Adv, Crosstalk)</li> </ul>
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## User Interface and Remote Control

The M8070B system software for the M8000 Series of BER test solutions is required to control the M8040A BERT.

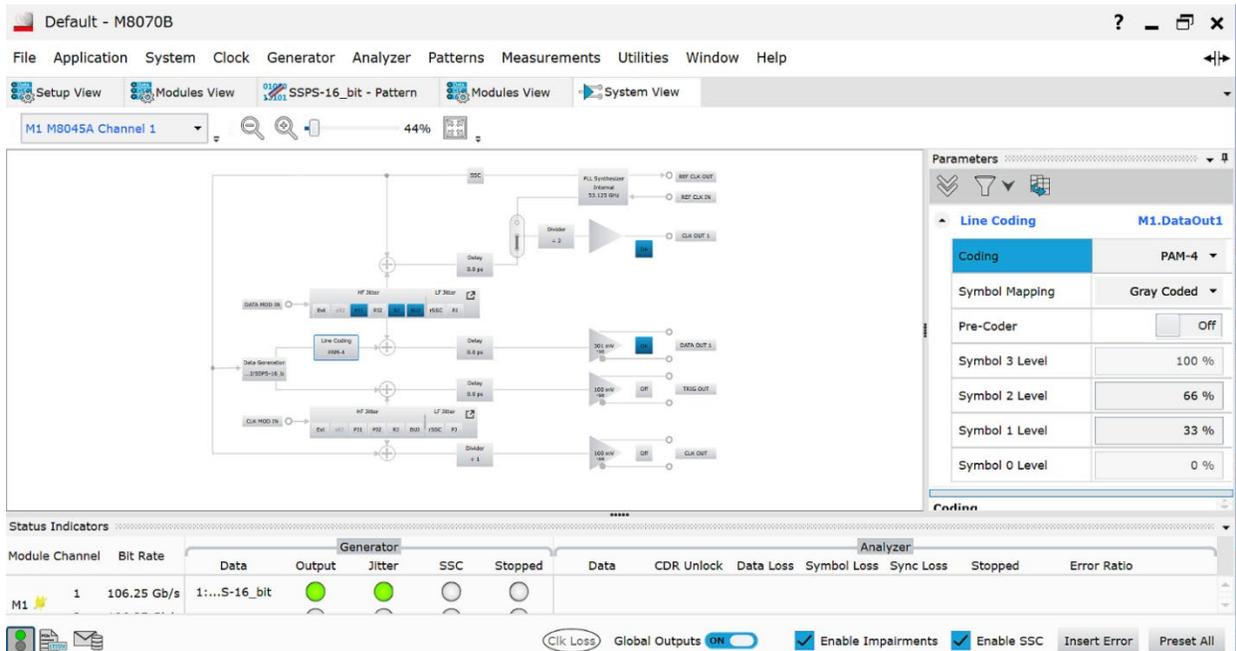


Figure 23. The graphical user interface offers multiple views that can be defined by the user. This example shows the system view on the left side and the pattern generator data output with the PAM4 coding and level linearity parameters at the right.

**Table 33. User interface and remote-control interface.**

System software	M8070B
Controller requirements	Embedded PC: Choose M8040A-BU1 or -BU3 for a pre-installed embedded controller M9537A including pre-installation of M8070B software and module licenses. M8040A-BU3 is pre-configured with Windows 10. Otherwise: M9537A 1-slot AXIe embedded controller, choose options for Windows 10, 8 or 16 GB RAM, SSD. External PC: USB connection recommended between external PC and AXIe chassis. Minimum of 8 GB RAM recommended. For PCIe connectivity please refer to list of tested PCs for AXIe Technical Note, pub no. 5990-7632EN
Operating system	Windows 10 (64 bit) Version 1607 (Anniversary Update) or newer (for detailed requirements refer to M8070B release notes). Microsoft Windows 7 (64 bit) SP1, Windows 8 (64 bit), Windows 8.1 (64 bit) are supported but not recommended.
Controller connectivity with AXIe chassis	USB 2.0 (Mini-B) recommended, PCIe 2.0/8x (only for highest data throughput and desktop PC)
Programming language	SCPI. Not compatible with N4900 Series and ParBERT 81250A
Remote control interface	Desktop or Laptop PC: LAN M9537A: LAN
Save/Recall	Yes
Software update	Under the help menu the M8070B can show if there are newer SW revisions of M8070B, M8070ADVB, M8070EDAB, and module driver packages available for download from K.com.
SCPI recorder <sup>1</sup>	Allows recording of the SCPI commands that correspond to the interactive control in the GUI. This includes: <ul style="list-style-type: none"> <li>• Parameter changes</li> <li>• Sequence and pattern configuration</li> <li>• Measurement creation, configuration and execution</li> <li>• Group configuration</li> <li>• Save and recall of settings</li> </ul> The recorded SCPI commands can be copied to the clipboard or saved to a file for later playback.
Display resolution	Minimum requirement 1024 x 768
Software pre-requisites	Microsoft Win 10, Keysight IO library rev. 17.2.20605 or above AXIe Chassis Firmware (Embedded System Module (ESM) from Keysight Technologies) version 1.3.42 or above. Microsoft Win 7 SP1 or 8 / 8.1 supported but not recommended.
Software download	See <a href="http://www.keysight.com/find/m8070b">http://www.keysight.com/find/m8070b</a> for latest version

1. M8070B V7.2 or higher, older versions included in M8070ADVB

**Table 34. Functions provides by the M8070ADVB advanced measurement software package.**

Advanced measurement	M8070ADVB
Measurements	See table measurements
Export of measurement results	Jitter tolerance results as *.csv file
Controlling other instruments via M8070B	External clock recovery units, e.g. N1076A, N1076B, N1077A, N1078A Real-time oscilloscopes, e.g. DASZ634A, UXR0334A
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as other test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device
DUT control interface	Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT
Auto-optimizing de-emphasis taps	DE taps are calculated for best eye height. Can be combined with embedding/de-embedding of s-parameter files. Supported DCA models: N1060A, N1094A/B, 86108B. Requires M8070B rev 6.7 or later.
Software pre-requisites	M8070B version 6.0 or later
License types	Choose between node-locked, transportable, network, USB-dongle license types either perpetual or time-based with 6/12/24 month duration. The network license is only recommended when using multiple M8040A setups within one company.

**Table 35. Functions provides by the Error Distribution Analysis software package M8070EDAB**

Error distribution analysis	M8070EDAB
Measurements	<ul style="list-style-type: none"> <li>• Frame loss ratio estimation</li> <li>• Error map</li> <li>• Symbol-errors per frame distribution</li> <li>• Consecutive error distance distribution</li> </ul>
Software pre-requisites	M8070B version 6.0 or later
License types	<p>You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with 6/12/24 month duration.</p> <p>The network license is only recommended when using multiple M8040A setups within one company</p>

## General Characteristics and Physical Dimensions Modules M8045A and M8046A

**Table 36. General characteristics for M8045A and M8046A modules.**

	M8045A	M8046A
Operating temperature	5 to 40 °C (41 to + 104 °F)	
Storage temperature	-40 to +70 °C (modules) (-40 to + 158 °F)	
Operating humidity	15 to 95% relative humidity at 40°C (non-condensing)	
Storage humidity	24 to 90% relative humidity at 65°C (non-condensing)	
Power requirements (module only) (W x H x D)	Single channel: 515 W Dual channel: 605 W	238 W
Physical dimensions for modules (W x H x D)	3-slot AXIe module: 351 x 92 x 315 mm (13.8 x 3.6 x 12.4 inch)	1-slot AXIe module: 351 x 30 x 309 mm (13.8 x 1.2 x 12.2 inch)
Physical dimensions for M8040A-BU1/-BU2 (W x H x D)	Installed in 5-slot AXIe chassis: 462 x 193 x 446 mm (18.2 x 7.6 x 17.6 inch)	
Weight net	M8045A module: single channel 6.9 kg (15.2 lb) M8045A dual channel: 7.5 kg (16.5 lb) With M8040A-BU1: 25 kg (55 lb) With M8040A-BU2: 21 kg (46.3 lb)	M8046A module: 3.6 kg (8.0 lb)  In bundle with M8045A and in a 5-slot chassis: 24.6 kg (54.3 lb)
Weight shipping	M8045A module: 11 kg (24 lb) With M8040A-BU1/-BU3: 37 kg (82 lb) With M8040A-BU2: 33 kg (73 lb)	M8046A module: 7.5 kg (16 lb) In bundle with M8045A and in a 5-slot chassis M9505A: 37.6 kg (83 lb), M9506A 23.5 kg (51.8 lb)
Recommend recalibration period	1 year	
Warm-up time	30 minutes	
Cooling requirements	Slot air flow direction is from right to left. When operating the M8045A /46A choose a location that provides at least 50 mm of clearance at each side. See also start-up guide for M9505/6A chassis.	
EMC	IEC 61326-1	
Safety	IEC 61010-1	
Quality	ISO 9001, 14001	

## Remote Head M8057A/B

Table 37. General characteristics for M8057A/B remote head.

M8057A/B	
Operating temperature	5 to 40 °C (41 to + 104 °F)
Storage temperature	−40 to +70 °C (modules) (−40 to + 158 °F)
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)
Physical dimensions (W x H x D)	Remote head 117 mm x 68 mm x 185 mm, (4.6" x 2.7" x 7.3")
Physical dimensions for remote head with cable	Length of cable connection between M8057A/B and M8045A module: 85 cm



Weight net	1.7 kg (3.75 lb)
Weight shipping	6.5 kg (14.4 lb)
Recommended recalibration period	1 year
Warm-up time	30 minutes
EMC	IEC 61326-1
Quality management	ISO 9001, 14001

## Specifications Assumptions

The specifications in this document describe the instruments' warranted performance. Non-warranted values are described as typical. All specifications are valid in the specified operating temperature range after the warm-up time and after auto-adjustment. If not otherwise stated all outputs need to be terminated with 50  $\Omega$  to GND. All M8045A specifications if not otherwise stated are valid at the end of the cable M8045A-801.

All M8046A specifications if not otherwise stated are valid using the recommended cable pair M8046A-802 (2.4 mm matched cable pair). Preliminary specifications are written in italics.

## Ordering of M8040A High-Performance BERT 64 Gbaud

The M8040A is scalable and upgradeable. The following table shows all available options. Upgrade options are shown below.

Description	Product #	Option	Comment
High-performance BERT 64 Gbaud (systemizing number for factory pre-installation)	M8040A		
<b>Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe</b>			
Pattern generator one channel NRZ, data rate up to 32 Gbaud (requires remote head, M8057A/B)	M8045A	G32	One of these is required
Pattern generator one channel NRZ, data rate up to 64 Gbaud (requires remote head, M8057A/B)	M8045A	G64	
Second channel, hardware and license (requires remote head, M8057A/B)	M8045A	0G2	
Advanced jitter sources for receiver characterization, module-wide license	M8045A	0G3	
De-emphasis, module-wide license	M8045A	0G4	
Reference clock multiplier, module-wide license	M8045A	0G6	
Forward Error Correction (FEC) encoding, module-wide license	M8045A	0G9	
PAM4 encoding up to 32 Gbaud, module-wide license	M8045A	0P3	
Extension to PAM4 encoding up to 64 Gbaud, module-wide license	M8045A	0P6	Only with G64, 0P3/UP3
Short cable 1.85 mm (m) to 1.85 mm (m), 0.15 m, absolute matching 699 ps ± 1 ps	M8045A	801	Qty 2 recommended
Remote head for M8045A pattern generator, 1 channel	M8057A		
<b>Analyzer module, 32/64 Gbaud, 1-slot AXIe</b>			
Analyzer, one channel, data rate up to 32 Gbaud, NRZ	M8046A	A32	
Analyzer, one channel, data rate up to 64 Gbaud, NRZ	M8046A	A64	
Equalization, license (only needed for > 32 Gbaud)	M8046A	0A3	Only with A64
PAM4 decoding up to 32 Gbaud, license	M8046A	0P3	
PAM4 decoding extension to 58 Gbaud, license	M8046A	0P6	Only with A64, 0P3, 0A3
Clock recovery for 32 Gbaud, license	M8046A	0A4	
Clock recovery extension to 64 Gbaud, license	M8046A	0A5	Only with A64 and 0A4
Interactive link training for PCIe, license	M8046A	0S1	Requires 0A4, 0G4
SKP OS filtering for PCIe and CCIX, license	M8046A	0S2	
Interactive link training for USB 3.2, license	M8046A	0S3	Requires 0A4
SKP OS filtering for USB 3.x, license	M8046A	0S4	Opt. 0A4 recommended
ALIGN filtering for SATA 3/6G, SAS 3/6/12G, license	M8046A	0S6	Opt. 0A4 recommended
PCIe Filtering of SKP OS Extension for 64 GT/s	M8046A	0N2	Opt. 0S2 required
Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m for clock input	M8046A	801	Qty 1 recommended
Matched cable pair 2.4 mm(m) to 2.4 mm (m)	M8046A	002	Qty 1 recommended
<b>Software and chassis</b>			
System software for M8000 Series	M8070B	unlicensed	
Advanced measurement package	M8070ADVB	1FP/1TP/ 1NP/1UP <sup>1</sup>	
Error distribution analysis package	M8070EDAB	1FP/1TP/ 1NP/1UP <sup>1</sup>	
5-slot AXIe chassis with USB option	M8040A	BU2	
5-slot AXIe chassis with USB option and embedded controller M9537A	M8040A	BU3	
<b>Warranty, calibration and productivity services</b>			

1. Multiple types of licenses are available. Choose between 6/12/24 month support subscriptions.

## M8040A upgrades

Description	Product #	Option	Comment
Upgrades for M8040A High-performance BERT 64 Gbaud	<b>M8040AU</b>		
<b>Pattern generator and clock module, 32/64 Gbaud, 3-slot AXIe</b>			
<b>M8045A</b>			
Upgrade to 64 Gbaud	M8045A	U64	License
Upgrade to second channel, hardware and license (requires remote head, M8057A/B)	M8045A	UG2	Requires return-to-factory
Upgrade to advanced jitter sources for receiver characterization, module-wide license	M8045A	UG3	License
Upgrade to de-emphasis, module-wide license	M8045A	UG4	License
Upgrade to Reference clock multiplier, module-wide license	M8045A	UG6	Requires return-to-factory for S/N <MYxxx01000
Upgrade to Forward Error Correction (FEC) encoding, module-wide license	M8045A	UG9	License
Upgrade to PAM4 encoding up to 32 Gbaud, module-wide license	M8045A	UP3	License
Upgrade to extension to PAM4 encoding up to 64 Gbaud, module-wide license	M8045A	UP6	Only with G64/U64/UP3
Remote head for M8045A pattern generator, 1 channel	M8057B		
<b>Analyzer module, 32/64 Gbaud, 1-slot AXIe</b>			
<b>M8046A</b>			
Upgrade M8046A for data rates up to 64 Gbaud, NRZ	M8046A	U64	Requires return-to-factory
Upgrade to equalization, license	M8046A	UA3	Only with A64/U64
Upgrade to PAM4 decoding up to 32 Gbaud, license	M8046A	UP3	License
Upgrade to PAM4 decoding extension to 58 Gbaud, license	M8046A	UP6	Requires return to factory for S/N < MYxxx02000
Upgrade to clock recovery 32 Gbaud, license	M8046A	UA4	Requires return to factory for S/N<DExxx01000
Upgrade to clock recovery extension to 64 Gbaud, license	M8046A	UA5	Only with A64/U64
Upgrade to interactive link training for PCIe, license	M8046A	US1	Requires -0A4/-UA4. Requires return to factory for S/N<MYxxx01000
Upgrade to SKP OS filtering for PCIe and CCIX, license	M8046A	US2	License
Upgrade to interactive link training for USB 3.2	M8046A	US3	License
Upgrade to SKP OS filtering for USB 3.x, license	M8046A	US4	License
Upgrade to ALIGN filtering for SATA/SAS and CCIX, license	M8046A	US6	License
Upgrade to PCIe Filtering of SKP OS Extension for 64 GT/s, license	M8046A	UN2	S/N > MYxxxx1000, -0S2/US2 required

Figure 24. All upgrade options for M8040A are orderable under M8040AU. Most options are license options, that can be upgraded on site

## Default accessories included with shipment

M8045A module: Four 50 $\Omega$ resistors, ESD protection kit, certificate of calibration, license entitlement certificate, no signal cables,
M8046A module: One bandpass filter for clock input, ESD protection kit, certificate of calibration, license entitlement certificate, one M8000 sync cable for LINK 1234 connection, no signal cables
M8057A/B remote head: includes cable connection to M8045A pattern generator module, one 50 $\Omega$ termination (2.4 mm)
M8040A-BU2: <b>M9505A AXIe chassis, USB cable, getting started guide, AXIe filler panel, power cord</b>
M8040A-BU3: M9505A AXIe chassis with embedded controller, Win 10 installed, USB cable, getting started guide, AXIe filler panel, power cord
M8070B: CD-ROM with M8070B system software

## Recommended accessories

Short cable, 1.85 mm (m) to 1.85 mm (m), 0.15 m, 699 ps delay $\pm$ 1 ps (two are recommended for each differential data output of M8057A/B)	M8045A-801
Matched cable pair 2.4 mm (m) to 2.4 mm (m), 2 ps, length 0.85 m (recommended for data input of M8046A analyzer)	M8046A-802
Cable 2.92 mm (m) to 2.92 mm (m), 0.5 m (recommended for clock input of M8046A analyzer)	M8046A-801
M8000 sync cable (when using the system clock of M8045A for M8046A) and LINK 1234 connection	M8051A-801
Attenuator, 6 dB, 1.85 mm	8490G-006
DC block 2.4 mm	N9398F
Matched directional coupler pair, 1 to 50 GHz, 13 dB, 2.4 mm (recommended for external interference source RI/SI)	M8045A-802
Matched coupler pair, DC to 40 GHz, 12 dB, 2.4 mm (recommended for PCIe)	M8045A-803
Bandpass filter 11.1 to 17.5 GHz, SMA (for M8046A clock input)	M8061A-803
Microwave pick-off tees, 2.4 mm, matched pair (Qty 1 is recommend for use with N1076A/77A)	N1027A-2P2
Microwave pick-off tees, 1.85 mm, matched pair (Qty 1 is recommend for use with N1076B/N1078A up to 32 Gbaud)	N1027A-2P8
Microwave pick-off tees, 1.0 mm, matched pair (Qty 1 is recommended for use with N1076B/N1078A above 32 Gbaud)	N1027A-2P1
Adapter 1.0 mm (m) to 1.85 mm (m) (Qty 2 is recommended for use with pick-off tees N1027A-2P1)	11921G
Adapter 1.0 mm (f) to 1.85 mm(f) (Qty 2 is recommended for connecting data cables to pick-off tee N1027A-2P1)	11921F
Adapter 2.4 mm (f) to 2.4 mm (f) (Qty 2 is recommended for connecting cables to pick-off tees)	11900B
Adapter 3.5 mm (m) to 3.5 mm (m) (Qty 2 is recommended for connecting pick-off tees directly to N1076A/77A inputs)	83059A
Adapter 2.94 mm(f) to 2.4 mm(m)	11904C
Adapter 2.94 mm(m) to 2.4 mm(f)	11904D
Rack-mount kit for AXIe 5-slot chassis M9505A	Y1226A
Optional 5 slot AXIe chassis, 300W / slot @ 220V power supply and Thunderbolt 3 connection	M9506A
PCI Express Re-driver recommended for PCI Express testing at 16 GT/s	M8047A

## Calibration, warranty, and productivity services

Calibration services (3 and 5 years)	R1282 (R-50C-011-3/-5)
Warranty extension to 3/5 years	R1280
Productivity assistance	R1380-M8000

## Related Keysight Literature

### Data sheets

<i>J-BERT M8020A - Data Sheet</i>	5991-3647EN
<i>M8030A Multi-channel BERT - Data Sheet</i>	5992-1287EN
<i>M8062A 32 Gb/s Front-end - Data Sheet</i>	5992-0987EN
<i>M9505A AXIe Chassis 5-slot - Data Sheet</i>	5990-6584EN
<i>M8196A 92 GSa/s AWG - Data Sheet</i>	5992-0971EN
<i>M8194A 120 GSa/s AWG - Data Sheet</i>	5992-3361EN
<i>M8054A Interference Source - Data Sheet</i>	5992-3971EN
<i>M8049A ISI Channel Boards - Data Sheet</i>	5992-3617EN
<i>N1085A PAM4 Measurement Application for 86100D DCA-X Series - Data Sheet</i>	5992-1248EN
<i>N1076A/N1076B/N1077A/N1078A Clock recovery - Data Sheet</i>	5992-1620EN
<i>N4917BSCA Optical Receiver Stress Test Solution IEEE 802.3bs - Data Sheet</i>	5992-2554EN
<i>N4891A 400GBase FEC-aware Receiver Test Solution - Data Sheet</i>	5992-4243EN
<i>A400GE-QDD 400GE Layer 1 BERT and KP4 FEC Multiport Test System – Data Sheet</i>	2020915-3908-01
<i>M8091BSPA IEEE802.3bs Receiver Test Pre-Compliance Application - Data Sheet</i>	5992-3288EN
<i>M809256PB OIF-CEI-56G Receiver Test Application - Data Sheet</i>	5992-3292EN
<i>M8091CKPA Pre-Compliance Receiver Test Application for IEEE 802.3ck - Data Sheet</i>	3120-1374.EN
<i>N5991 Receiver Compliance Test Automation Platform – Data Sheet</i>	5992- 4365EN
<i>M8047A Redriver for PCIe - Data Sheet</i>	3120-1399.EN

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## Application notes, white papers and posters

<i>Characterizing and verifying compliance of 100Gb Ethernet components and systems - Application Note</i>	5992-0019EN
<i>Master 400G - Poster</i>	5992-2143EN
<i>Equalization: The correction and analysis of degraded signals - White Paper</i>	5989-3777EN
<i>BER measurement using a real-time Oscilloscope controlled from M8070A system software - Application Note</i>	5992-2676EN
<i>Advanced modulation and coding challenges - White Paper</i>	5992-3021EN
<i>Error analysis of PAM4 signals - Application Note</i>	5991-3724EN

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