R&S®RTO6
OSCILLOSCOPE SERIES

Specifications



Specifications
Version 16.00

ROHDE&SCHWARZ
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CONTENTS

Definitions **5**

Base unit **6**

Vertical system 6

Horizontal system 9

Acquisition system 9

Differential signals 11

High definition mode 11

Trigger system 12

RF characteristics 14

Waveform measurements 15

Mask testing 17

Waveform math 18

Spectrum analysis 18

Search and mark function 19

Display characteristics 19

Input and output 19

General data **21**

Options **23**

R&S®RTO6-B1 mixed signal option 23

Vertical system *23*

Horizontal system *23*

Acquisition system *23*

Trigger system *23*

Waveform measurements *24*

Display characteristics *24*

R&S®RTO6-B6 arbitrary waveform generator 25

Analog channels *25*

8 bit pattern generator *27*

R&S®RTO6-B7 16 GHz differential pulse source 28

Output *28*

DC characteristics *28*

Time domain characteristics *28*

Frequency domain characteristics *29*

General *29*

R&S®RTO6-B10 GPIB interface 29

R&S®RTO6-B19 replacement solid state disk 29

R&S®RTO6-K11 I/Q software interface 29

R&S®RTO6-K12 jitter analysis 30

R&S®RTO6-K13 clock data recovery 31

R&S®RTO6-K21 USB 2.0 compliance test 32
R&S®RTO6-K22 Ethernet compliance test (10/100/1000BASE-T/EEE) 33
R&S®RTO6-K23 Ethernet compliance test (2.5/5/10GBASE-T) 34
R&S®RTO6-K24 Ethernet compliance test (100BASE-T1) 35
R&S®RTO6-K26 MIPI D-PHY compliance test 36
R&S®RTO6-K27 MIPI D-PHY 2.5 compliance test 38
R&S®RTO6-K31 power analysis 40
R&S®RTO6-K37 spectrogram 41
R&S®RTO6-K39 user-defined math 41
R&S®RTO6-K81 PCI Express 1.1/2.0 compliance test 41
R&S®RTO6-K87 Ethernet compliance test (1000BASE-T1) 42
R&S®RTO6-K88 Ethernet compliance test (MGBASE-T1) 42
R&S®RTO6-K89 Ethernet compliance test (10BASE-T1) 42
R&S®RTO6-K91 DDR3/DDR3L/LPDDR3 signal integrity debug and compliance test 43
R&S®RTO6-K92 eMMC compliance test 46
R&S®RTO6-K99 R&S®ScopeSuite automation 46
R&S®RTO6-K121 deembedding base option 47
Proven cable/proven probe *47*
R&S®RTO6-K126 embedding and equalization option 47
R&S®RTO6-K130 TDR/TDT analysis 48
R&S®RTO6-K133 advanced jitter analysis 49
R&S®RTO6-K134 advanced jitter and noise analysis 50
R&S®RTO6-K135 PAM-N analysis 51
R&S®RTO6-K136 advanced eye analysis 52
R&S®RTO6-K155 EMC/ESD analysis 52
R&S®RTO6-K500 bus analysis 53
R&S®RTO6-K510 low-speed serial busses triggering and decoding 53
I^2C triggering and decoding *53*
SPI triggering and decoding *54*
UART/RS-232/RS-422/RS-485 triggering and decoding *54*
I^2S triggering and decoding *55*
Manchester and NRZ triggering and decoding *55*
R&S®RTO6-K520 automotive protocols triggering and decoding 56
CAN/CAN FD triggering and decoding *56*
CAN XL triggering and decoding *57*
LIN triggering and decoding *58*
FlexRay triggering and decoding *59*
SENT triggering and decoding *59*
CXPI triggering and decoding *60*
R&S®RTO6-K530 aerospace protocols triggering and decoding 61

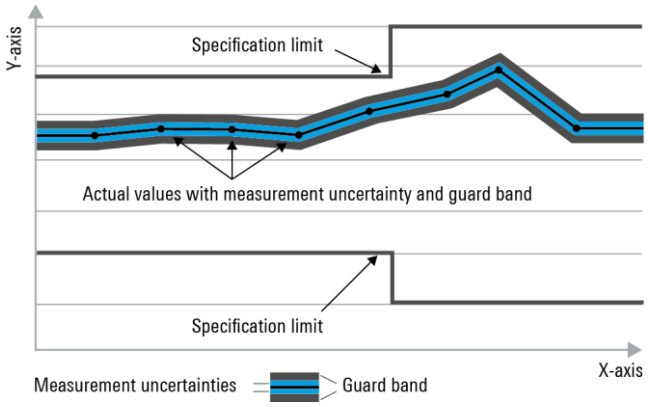
MIL-STD-1553 triggering and decoding *61*
ARINC 429 triggering and decoding *61*
SpaceWire triggering and decoding *62*
R&S®RTO6-K540 Ethernet protocols triggering and decoding 62
Ethernet (10BASE-T/100BASE-TX) triggering and decoding *62*
MDIO triggering and decoding *63*
R&S®RTO6-K550 MIPI low speed triggering and decoding 63
RFFE triggering and decoding *63*
I^3C triggering and decoding *65*
R&S®RTO6-K560 automotive Ethernet triggering and decoding 66
Ethernet (10BASE-T1S) triggering and decoding *66*
Ethernet (100BASE-T1) triggering and decoding *67*
Ethernet (1000BASE-T1) triggering and decoding *68*
R&S®RTO6-K570 USB protocols triggering and decoding 68
USB 1.0/1.1/2.0 triggering and decoding *68*
USB 3.1 Gen 1 triggering and decoding *69*
USB power delivery triggering and decoding *70*
USB 3.1 SSIC triggering and decoding *71*
R&S®RTO6-K580 MIPI high speed triggering and decoding 71
MIPI D-PHY triggering and decoding *71*
MIPI M-PHY triggering and decoding *72*
R&S®RTO6-K590 PCI express triggering and decoding 73
8b10b triggering and decoding *73*
PCI Express 1.1/2.0 triggering and decoding *73*
Ordering information 75
Warranty and service 77

Definitions

General
Product data applies under the following conditions:

- Three hours of storage at ambient temperature followed by 30 minutes of warm-up operation
- Specified environmental conditions met
- Recommended calibration interval adhered to
- All internal automatic adjustments performed, if applicable

Specifications with limits
Represent warranted product performance by means of a range of values for the specified parameter. These specifications are marked with limiting symbols such as <, ≤, >, ≥, ± or descriptions such as maximum, limit of, minimum. Compliance is ensured by testing or is derived from the design. Test limits are narrowed by guard bands to take into account measurement uncertainties, drift and aging, if applicable.



Non-traceable specifications with limits (n. trc.)
Represent product performance that is specified and tested as described under “Specifications with limits” above. However, product performance in this case cannot be warranted due to the lack of measuring equipment traceable to national metrology standards. In this case, measurements are referenced to standards used in the Rohde & Schwarz laboratories.

Specifications without limits
Represent warranted product performance for the specified parameter. These specifications are not specially marked and represent values with no or negligible deviations from the given value, e.g. dimensions or resolution of a setting parameter. Compliance is ensured by design.

Typical data (typ.)
Characterizes product performance by means of representative information for the given parameter. When marked with <, > or as a range, it represents the performance met by approximately 80 % of the instruments at production time. Otherwise, it represents the mean value.

Nominal values (nom.)
Characterize product performance by means of a representative value for the given parameter, e.g. nominal impedance. In contrast to typical data, a statistical evaluation does not take place and the parameter is not tested during production.

Measured values (meas.)
Characterize expected product performance by means of measurement results gained from individual samples.

Uncertainties
Represent limits of measurement uncertainty for a given measurand. Uncertainty is defined with a coverage factor of 2 and has been calculated in line with the rules of the Guide to the Expression of Uncertainty in Measurement (GUM), taking into account environmental conditions, aging, wear and tear.

Device settings and GUI parameters are designated with the format “parameter: value”.

Non-traceable specifications with limits, typical data as well as nominal and measured values are not warranted by Rohde & Schwarz.

In line with the 3GPP standard, chip rates are specified in million chips per second (Mcps), whereas bit rates and symbol rates are specified in billion bit per second (Gbps), million bit per second (Mbps), thousand bit per second (kbps), million symbols per second (Msps) or thousand symbols per second (ksps), and sample rates are specified in million samples per second (Msample/s). Gbps, Mcps, Mbps, Msps, kbps, ksps and Msample/s are not SI units.

Base unit

Vertical system

Input channels		4 channels
Input impedance		50 Ω ± 2.5 %, 50 Ω ± 1.5 % (typ.), 1 MΩ ± 1 % || 15 pF (meas.)
Analog bandwidth (–3 dB)	at 50 Ω input impedance	
	instrument bandwidth 600 MHz (R&S®RTO6-B90 option)	≥ 600 MHz
	instrument bandwidth 1 GHz (R&S®RTO6-B91 option)	≥ 1 GHz
	instrument bandwidth 2 GHz (R&S®RTO6-B92 option)	≥ 2 GHz
	instrument bandwidth 3 GHz (R&S®RTO6-B93 option)	≥ 3 GHz
	instrument bandwidth 4 GHz (R&S®RTO6-B94 option)	≥ 4 GHz
	instrument bandwidth 6 GHz (R&S®RTO6-B96 option)	≥ 6 GHz on 2 channels [1], ≥ 4 GHz on 4 channels
	at 1 MΩ input impedance	≥ 500 MHz (meas.)
Bandwidth limit filters	at 50 Ω input impedance	
	R&S®RTO6-B90, R&S®RTO6-B91, R&S®RTO6-B92, R&S®RTO6-B93, R&S®RTO6-B96 options	brick wall (maximally flat), Gaussian (step-response optimized)
	R&S®RTO6-B94 option	brick wall
	at 1 MΩ input impedance	brick wall
Analog bandwidth limits	max. –1.5 dB, min. –4 dB	200 MHz, 20 MHz
Rise/fall time	10 % to 90 % at 50 Ω, bandwidth limit Gaussian, except R&S®RTO6-B94 option brick wall (meas.)	
	R&S®RTO6-B90 option	528 ps
	R&S®RTO6-B91 option	319 ps
	R&S®RTO6-B92 option	188 ps
	R&S®RTO6-B93 option	135 ps
	R&S®RTO6-B94 option	104 ps
	R&S®RTO6-B96 option	77 ps
Input VSWR	input frequency	R&S®RTO6-B90, R&S®RTO6-B91, R&S®RTO6-B92, R&S®RTO6-B93, R&S®RTO6-B94 options
	≤ 2 GHz	1.25 (meas.)
	> 2 GHz	1.4 (meas.)
	input frequency	R&S®RTO6-B96 option
	≤ 2 GHz	1.25 (meas.)
	> 2 GHz to ≤ 4 GHz	1.6 (meas.)
	> 4 GHz	2.0 (meas.)
Vertical resolution		16 bit system architecture
Effective number of bits (meas.)	at 50 Ω, 50 mV/div, 10 MHz input signal with 90 % full-scale	
	50 MHz	9.4
	100 MHz	9.0
	200 MHz	8.6
	300 MHz	8.2
	500 MHz	8.1
	1 GHz	7.7
	2 GHz	7.1
	4 GHz	6
	6 GHz	6.1
DC gain accuracy	offset and position set to 0 V, after self-alignment	
	at 50 Ω, input sensitivity > 5 mV/div	±1.5 %
	at 50 Ω, input sensitivity ≤ 5 mV/div	±2 %
	at 1 MΩ	±2 %
Input coupling	at 50 Ω	DC, GND
	at 1 MΩ	DC, AC (> 7 Hz), GND

[1] Two channels means either channel 1 or channel 2 and either channel 3 or channel 4.

Input sensitivity	at 50 Ω	1 mV/div to 1 V/div, entire analog bandwidth supported for all input sensitivities
	at 1 MΩ	1 mV/div to 10 V/div, entire analog bandwidth supported for all input sensitivities
Maximum input voltage	at 50 Ω	5 V (RMS)
	at 1 MΩ	150 V (RMS), 200 V (V_p), derates at 20 dB/decade to 5 V (RMS) above 250 kHz
	at 1 MΩ with R&S®RT-ZP10 passive probe	400 V (RMS), 1650 V (V_p), 300 V (RMS) CAT II; for derating and details, see R&S®RT-Zxx Standard Probes specifications (PD 3607.3851.22)
Position range		±5 div
Offset range at 50 Ω	input sensitivity	
	> 316 mV/div to ≤ 1 V/div	±10 V
	> 100 mV/div to ≤ 316 mV/div	±3 V
	1 mV/div to ≤ 100 mV/div	±1 V
Offset range at 1 MΩ	input sensitivity	
	> 3.16 V/div to ≤ 10 V/div	±(115 V – input sensitivity × 5 div)
	> 1 V/div to ≤ 3.16 V/div	±100 V
	> 316 mV/div to ≤ 1 V/div	±(11.5 V – input sensitivity × 5 div)
	> 100 mV/div to ≤ 316 mV/div	±10 V
	> 31.6 mV/div to ≤ 100 mV/div	±(1.15 V – input sensitivity × 5 div)
	1 mV/div to ≤ 31.6 mV/div	±1 V
Offset accuracy		±(0.35 % × |net offset| + 2.5 mV + 0.1 div × input sensitivity) (net offset = offset – position × input sensitivity)
DC measurement accuracy	after adequate suppression of measurement noise using high-resolution sampling mode, waveform averaging or a combination of both	±(DC gain accuracy × |reading – net offset| + offset accuracy)
Channel-to-channel isolation (each channel at same input sensitivity)	input frequency within instrument bandwidth	
	≤ 2 GHz	> 60 dB
	> 2 GHz to ≤ 4 GHz	> 50 dB
	> 4 GHz to ≤ 6 GHz	> 40 dB

RMS noise floor at instrument bandwidth at 50 Ω (typ.) (bandwidth limit brick wall)	input sensitivity		R&S®RTO6-B90 option	R&S®RTO6-B91 option
	1 mV/div		0.06 mV	0.09 mV
	2 mV/div		0.07 mV	0.09 mV
	5 mV/div		0.10 mV	0.12 mV
	10 mV/div		0.17 mV	0.20 mV
	20 mV/div		0.32 mV	0.37 mV
	50 mV/div		0.86 mV	0.93 mV
	100 mV/div		1.60 mV	1.79 mV
	200 mV/div		2.87 mV	3.53 mV
	500 mV/div		6.20 mV	8.76 mV
	1 V/div		10.9 mV	17.2 mV
	input sensitivity		R&S®RTO6-B92 option	R&S®RTO6-B93 option
	1 mV/div		0.13 mV	0.18 mV
	2 mV/div		0.13 mV	0.19 mV
	5 mV/div		0.16 mV	0.21 mV
	10 mV/div		0.26 mV	0.33 mV
	20 mV/div		0.49 mV	0.60 mV
	50 mV/div		1.18 mV	1.49 mV
	100 mV/div		2.37 mV	2.89 mV
	200 mV/div		4.68 mV	5.95 mV
	500 mV/div		12.1 mV	15.3 mV
	1 V/div		24.1 mV	29.7 mV
	input sensitivity		R&S®RTO6-B94 option	R&S®RTO6-B96 option
	1 mV/div		0.20 mV	0.30 mV
	2 mV/div		0.21 mV	0.30 mV
	5 mV/div		0.25 mV	0.31 mV
	10 mV/div		0.38 mV	0.43 mV
	20 mV/div		0.67 mV	0.73 mV
	50 mV/div		1.66 mV	1.73 mV
	100 mV/div		3.23 mV	3.26 mV
	200 mV/div		6.65 mV	6.68 mV
	500 mV/div		17.1 mV	17.3 mV
	1 V/div		34.2 mV	34.5 mV
RMS noise floor at instrument bandwidth at 1 MΩ (meas.)	input sensitivity			
	1 mV/div		0.13 mV	
	2 mV/div		0.13 mV	
	5 mV/div		0.17 mV	
	10 mV/div		0.24 mV	
	20 mV/div		0.43 mV	
	50 mV/div		1.1 mV	
	100 mV/div		2.1 mV	
	200 mV/div		4.4 mV	
	500 mV/div		10 mV	
	1 V/div		20 mV	
	2 V/div		44 mV	
	5 V/div		105 mV	
	10 V/div		210 mV	
RMS noise floor for HD mode at 50 Ω (meas.)	bandwidth	input sensitivity		
		1 mV/div	10 mV/div	100 mV/div
	10 MHz	10 µV	18 µV	150 µV
	100 MHz	31 µV	56 µV	470 µV
	500 MHz	63 µV	110 µV	960 µV
	1 GHz	92 µV	170 µV	1.41 mV
	2 GHz	140 µV	220 µV	1.78 mV

Horizontal system

Timebase range		25 ps/div to 10 000 s/div, settable to any value within range
Reference position	horizontal position of trigger point	0 % to 100 % of measurement display area
Horizontal position range	max.	+(memory depth/current sampling rate)
	min.	–10 000 s
Horizontal modes	normal mode	if timebase < 1 s/div (default value) or roll mode = off
	roll mode	The aquired waveform points are continuously scrolled from the right to the left of the display. Sample rates up to 20 Msample/s with a maximum record length of 40 Mpoints are supported.
Channel-to-channel skew		< 100 ps (meas.)
Deskew range		±100 ns
Timebase accuracy	after delivery/calibration, at +23 °C	±10 ppb
	during calibration interval	±100 ppb
	long-term stability (more than one year since calibration)	±(50 + 50 × years since calibration) ppb
Sample clock jitter	acquired time range	RMS value (meas.)
	10 µs	72 fs
	100 µs	85 fs
	1 ms	93 fs
	10 ms	169 fs
Intrinsic jitter	RMS value	300 fs (meas.)
Time interval error (TIE)	RMS values	$\sqrt{(\mathrm{Noise/SlewRate})^2 + (\mathrm{IntrinsicJitter})^2}$
Periodic jitter	RMS values	$\sqrt{2}\sqrt{(\mathrm{Noise/SlewRate})^2 + (\mathrm{Intrinsic\,Jitter})^2}$
Cycle-to-cycle jitter	RMS values	$\sqrt{3}\sqrt{(\mathrm{Noise/SlewRate})^2 + (\mathrm{Intrinsic\,Jitter})^2}$
Delta time accuracy	intra-channel, peak-peak, ±5 sigma	$\pm\left(5 \cdot \sqrt{\mathrm{TIE_{edge1}}^2 + \mathrm{TIE_{edge2}}^2} + \mathrm{timebase\,accuracy} \cdot \mathrm{delta\,time}\right)$

Acquisition system

Realtime sampling rate	R&S®RTO6-B90, R&S®RTO6-B91, R&S®RTO6-B92, R&S®RTO6-B93 options	max. 10 Gsample/s on each channel
	R&S®RTO6-B94, R&S®RTO6-B96 options	max. 10 Gsample/s on 4 channels, max. 20 Gsample/s on 2 channels
Realtime waveform acquisition rate	max.	> 1 000 000 waveforms/s
Memory depth [2]	standard	200 Mpoints on 4 channels, 400 Mpoints on 2 channels, 800 Mpoints on 1 channel
	R&S®RTO6-B104 option	400 Mpoints on 4 channels, 800 Mpoints on 2 channels (restriction: 400 Mpoints on 2 channels when channel 1 and channel 2 or channel 3 and channel 4 are turned on), 800 Mpoints on 1 channel
	R&S®RTO6-B110 option	1 Gpoint on 4 channels, 2 Gpoints on 2 channels (restriction: 1 Gpoint on 2 channels when channel 1 and channel 2 or channel 3 and channel 4 are turned on), 2 Gpoints on 1 channel

[2] The maximum available memory depth depends on the bit depth of the acquired data and, therefore, on the settings of the acquisition system, such as decimation mode, waveform arithmetic, number of waveform streams or high definition mode.

Realtime digital filters	selectable filter for the data acquisition and/or the trigger system	
	lowpass filter	cutoff frequency selectable up to 50 % of analog bandwidth: 100 kHz, 200 kHz, 300 kHz, 500 kHz, 1 MHz, 2 MHz, 3 MHz, 5 MHz, 10 MHz, 20 MHz, 30 MHz, 50 MHz, 100 MHz, 500 MHz, 1 GHz
		additionally 2 GHz cutoff frequency for 20 Gsample/s realtime sampling rate (R&S®RTO6-B94, R&S®RTO6-B96 options)
Decimation modes	sample	first sample in decimation interval
	peak detect	largest and smallest sample in decimation interval
	high resolution	average value of samples in decimation interval
	root mean square	root of squared average of samples in decimation interval
Waveform arithmetic	off	no arithmetic
	envelope	envelope of acquired waveforms
	average	average of acquired waveforms, max. average depth depends on decimation mode [3]
	sample	max. 16 777 215
	high resolution	max. 65 535
	root mean square	max. 255
	reset condition	no reset (standard), reset by time, reset by number of processed waveforms
Waveform streams per channel		up to 3 with independent selection of decimation mode and waveform arithmetic
Sampling modes	realtime mode	max. sampling rate set by digitizer
	interpolated time	enhancement of sampling resolution by interpolation; max. equivalent sampling rate is 4 Tsample/s
Interpolation modes		linear, sin(x)/x, sample & hold
Fast segmentation mode	continuous recording of waveforms in acquisition memory without interruption due to visualization	
	max. realtime waveform acquisition rate	> 2 500 000 waveforms/s
	min. blind time between consecutive acquisitions	< 300 ns
	max. recordable acquisitions	up to 1.5 million acquisitions, depending on instrument settings and memory option (R&S®RTO6-B104/-B110)
History mode	accesses previous acquisitions for further analysis.	
	max. recordable acquisitions	up to 1.5 million acquisitions, depending on instrument settings and memory option (R&S®RTO6-B104/-B110)
	analysis functions	same as for the waveform of the latest acquisition: waveform measurements, mask testing, waveform math, search and mark functions, zoom and others
	history player	shows one history acquisition after the other for a user definable display time (40 µs to 10 s)
	timestamp formats	timestamp of each acquisition: absolute (date and time) or relative to latest acquisition
	save options	all history acquisitions or a user definable subset

[3] Waveform averaging is not compatible with peak detect decimation.

Differential signals

General description	Calculation of differential and common mode signals from p part and n part connected to separate input channels. The R&S®RTO64 digital trigger concept enables these signals to be used as a trigger input.	
Input channels		channel 1, channel 2, channel 3, channel 4
Differential signal	difference between two input channels	channel 1 and channel 2, channel 3 and channel 4
Common mode signal	sum of two input channels	channel 1 and channel 2, channel 3 and channel 4
Maximum number of outputs	differential signals	2
	common mode signals	2

High definition mode

General description	The high definition mode increases the numeric resolution of waveform signals with digital filtering to reduce noise. The signals with increased numeric resolution are used as a triggering input thanks to the R&S®RTO64 digital trigger concept.	
Numeric resolution	R&S®RTO6-B90, R&S®RTO6-B91, R&S®RTO6-B92, R&S®RTO6-B93, R&S®RTO6-B94	
	bandwidth	resolution
	10 kHz to 50 MHz	16 bit
	100 MHz	14 bit
	200 MHz	13 bit
	300 MHz	12 bit
	500 MHz	12 bit
	1 GHz	10 bit
	R&S®RTO6-B96 options (2 channels)	
	bandwidth	resolution
	10 kHz to 200 MHz	16 bit
	300 MHz	12 bit
	500 MHz	12 bit
	1 GHz	11 bit
	2 GHz	10 bit
	R&S®RTO6-B96 options (4 channels)	
	bandwidth	resolution
	10 kHz to 50 MHz	16 bit
	100 MHz	14 bit
	200 MHz	13 bit
	300 MHz	12 bit
	500 MHz	12 bit
	1 GHz	10 bit
Realtime sampling rate	R&S®RTO6-B90, R&S®RTO6-B91, R&S®RTO6-B92, R&S®RTO6-B93, R&S®RTO6-B94, R&S®RTO6-B96 options (4 channels)	max. 5 Gsample/s on each channel
	R&S®RTO6-B94, R&S®RTO6-B96 options (2 channels)	max. 10 Gsample/s on each channel
Input sensitivity		input sensitivity range extends down to 500 µV/div; 500 µV/div is a magnification of 1 mV/div setting.

Trigger system

Sources		channel 1, channel 2, channel 3, channel 4, inverted channels, external trigger, differential, common mode
Trigger bandwidth	max.	same bandwidth as analog bandwidth for all vertical scales and trigger types
	user-defined	cutoff frequency selectable up to 50 % of analog bandwidth: 100 kHz, 200 kHz, 300 kHz, 500 kHz, 1 MHz, 2 MHz, 3 MHz, 5 MHz, 10 MHz, 20 MHz, 30 MHz, 50 MHz, 100 MHz, 500 MHz, 1 GHz
		additional 2 GHz cutoff frequency for 20 Gsample/s realtime sampling rate (R&S®RTO6-B94, R&S®RTO6-B96 options)
Trigger sensitivity		0.0001 div, from DC to analog bandwidth for all vertical scales and trigger types
Trigger hysteresis	modes	auto (standard) or manual
	sensitivity	0.0001 div, from DC to analog bandwidth for all vertical scales and trigger types
Trigger jitter	full-scale sine wave of frequency set to –3 dB bandwidth	< 1 ps (RMS) (meas.)
Sweep mode		auto, normal, single, n single
Event rate	max.	one event for every 400 ps time interval
Trigger level range	internal	±5 div from center of screen
	external	see “external trigger input”
Holdoff range	time	100 ns to 10 s, fixed and random
	events	1 event to 2 000 000 000 events

Main trigger modes		
Edge	triggers on specified slope (positive, negative or either) and level	
Glitch	triggers on glitches of positive, negative or either polarity that are shorter or longer than specified width	
	glitch width	100 ps to 1000 s
		50 ps to 1000 s (R&S®RTO6-B94, R&S®RTO6-B96 options)
Width	triggers on positive or negative pulse of specified width; width can be shorter, longer, inside or outside the interval	
	pulse width	100 ps to 1000 s
		50 ps to 1000 s (R&S®RTO6-B94, R&S®RTO6-B96 options)
Runt	triggers on pulse of positive, negative or either polarity that crosses one threshold but fails to cross a second threshold before recrossing the first one; runt pulse width can be arbitrary, shorter, longer, inside or outside the interval	
	runt pulse width	100 ps to 1000 s
		50 ps to 1000 s (R&S®RTO6-B94, R&S®RTO6-B96 options)
Window	triggers when signal enters or exits a specified voltage range; triggers also when signal stays inside or outside the voltage range for a specified period of time	
Timeout	triggers when signal stays high, low or unchanged for a specified period of time	
	timeout	100 ps to 1000 s
		50 ps to 1000 s (R&S®RTO6-B94, R&S®RTO6-B96 options)
Interval	triggers when time between two consecutive edges of same slope (positive or negative) is shorter, longer, inside or outside a specified range	
	interval time	100 ps to 1000 s
		50 ps to 1000 s (R&S®RTO6-B94, R&S®RTO6-B96 options)

Slew rate	triggers when the time required by a signal edge to toggle between user-defined upper and lower voltage levels is shorter, longer, inside or outside the interval; edge slope may be positive, negative or either	
	toggle time	100 ps to 1000 s
		50 ps to 1000 s (R&S®RTO6-B94, R&S®RTO6-B96 options)
Data2clock	triggers on setup time and hold time violations between clock and data present on any two input channels; users can specify monitored time interval ranging from –100 ns to 100 ns around a clock edge and must be at least 100 ps wide	
Pattern	triggers when a logical combination (and, nand, or, nor) of the input channels stays true for a period of time shorter, longer, inside or outside a specified range	
State	triggers when a logical combination (and, nand, or, nor) of the input channels stays true at a slope (positive, negative or either) in one selected channel	
Serial pattern	triggers on serial data pattern up to 128 bit clocked by one input channel; pattern bits may be high (H), low (L) or don't care (X); clock edge slope may be positive, negative or either; hardware CDR selectable as clock source (requires R&S®RTO6-K13 option)	
	max. data rate	< 2.50 Gbps
		< 5 Gbps (R&S®RTO6-B94, R&S®RTO6-B96 options)
TV/video	triggers on baseband analog progressive and interlaced video signals including NTSC, PAL, PAL-M, SECAM, EDTV and HDTV broadcast standards as well as custom bi-level and tri-level sync video standards	
	trigger modes	all fields, odd fields, even fields, all lines, line number

Advanced trigger modes		
Zone trigger	triggers on user-defined zones drawn on the display	
	source	acquired waveforms (input channels), math waveforms
	number of zones	up to 8
	zone shapes	rectangles, polygones
	zone types	must intersect, must not intersect
	combination of zones	logical combination of zones of multiple sources using Boolean expressions
	trigger compatibility	compatible with the edge, glitch, width, runt, window, timeout, interval, slew rate, data2clock, pattern, state, serial pattern, trigger qualification, and sequence trigger modes
Trigger qualification	trigger events may be qualified by a logical combination of unused channels	
	qualifiable events	edge, glitch, width, runt, window, timeout, interval
Sequence trigger (A/B/R trigger)	triggers on B event after occurrence of A event; delay condition after A event specified either as time interval or number of B events; an optional R event resets the trigger sequence to A	
	A event	any trigger mode
	B event	edge, glitch, width, runt, window, timeout, interval, slew rate
	R event	edge, glitch, width, runt, window, timeout, interval, slew rate
Serial bus trigger	optional	see dedicated triggering and decoding options
NFC trigger		with R&S®RTO6-K11 option

CDR trigger	triggers on clock signal recovered from the trigger source signal; phase of the trigger instant user-selectable as fraction of bit period; requires R&S®RTO6-K13 option	
	CDR configuration parameters	PLL order (first or second), nominal bit rate, loop bandwidth, relative bandwidth, damping factor, unit interval offset
	CDR bit rate range	
	R&S®RTO6-B90, R&S®RTO6-B91, R&S®RTO6-B92, R&S®RTO6-B93 options	200 kbps to 2.5 Gbps
	R&S®RTO6-B94, R&S®RTO6-B96 options	200 kbps to 2.5 Gbps standard, 400 kbps to 5.0 Gbps when operating at 20 Gsample/s realtime sampling rate [4]
External trigger input	input impedance	50 Ω (nom.) or 1 MΩ (nom.) || 20 pF (meas.)
	max. input voltage at 50 Ω	5.5 V (peak)
	max. input voltage at 1 MΩ	30 V (RMS) derates at 20 dB/decade to 5 V (RMS) above 25 MHz
	max. trigger level	±5 V
	sensitivity	
	input frequency ≤ 100 MHz	300 mV (peak-to-peak) (meas.)
	100 MHz < input frequency ≤ 500 MHz	600 mV (peak-to-peak) (meas.)
	input coupling	AC, DC (50 Ω and 1 MΩ), GND, HF reject (attenuates > 50 kHz or > 50 MHz, user-selectable), LF reject (attenuates < 5 kHz or < 50 kHz, user-selectable)
	trigger modes	edge (rise or fall)
Trigger out	functionality	a pulse is generated for every acquisition trigger event
	output voltage	0 V to 5 V at high impedance; 0 V to 2.5 V at 50 Ω
	pulse width	selectable between 50 ns and 60 ms
	pulse polarity	low active or high active
	output delay	depends on trigger settings
	jitter	±600 ps (RMS) (meas.)

RF characteristics [5]

Sensitivity/noise density	at 1.001 GHz (measurement of the power spectral density at 1.001 GHz at input sensitivity 1 mV/div, corresponding to –36 dBm input range of the oscilloscope, using the FFT with center frequency 1.001 GHz, span 500 kHz, RBW 3 kHz)	–160 dBm (1 Hz) (meas.)
Noise figure	at 1.001 GHz (calculated based on the noise density above)	14 dB (meas.)
Dynamic range	measured for an input carrier with frequency 1 GHz and level –1 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 1 GHz, span 100 MHz, RBW 400 Hz at +20 MHz from the center frequency	109 dB (meas.)
Absolute amplitude accuracy	0 Hz to 5 GHz	±1 dB (meas.)
Phase noise (meas.)	at 1 GHz	
	10 kHz offset	–122 dBc (1 Hz)
	100 kHz offset	–126 dBc (1 Hz)

[4] The frontends of the R&S®RTO6-B94 and the R&S®RTO6-B96 sample at 20 Gsample/s when at most one channel of each pair {channel1, channel2} and {channel3, channel4} is active; and the user-selected sampling resolution in realtime sampling mode or interpolated time sampling mode is 50 ps or smaller.

[5] The RF characteristics are measured for the R&S®RTO6-B96 option with 6 GHz bandwidth.

EVM (meas.)	802.11ax, 2.4 GHz carrier, bandwidth 20 MHz, 64QAM	0.7 % (–43 dB)
	5G NR, 3.5 GHz carrier, bandwidth 20 MHz, QPSK	0.78 % (–42 dB)
	5G NR, 3.5 GHz carrier, bandwidth 100 MHz, QPSK	1 % (–40 dB)
Spurious-free dynamic range (excl. harmonics)	measured for an input carrier with frequency 950 MHz and level 0 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 2 GHz, span 4 GHz, RBW 100 kHz	67 dBc (meas.)
Second harmonic distortion	measured for an input carrier with frequency 950 MHz and level 0 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 950 MHz, span 4 GHz, RBW 100 kHz	–52 dBc (meas.)
Third harmonic distortion	measured for an input carrier with frequency 950 MHz and level 0 dBm at input sensitivity 70 mV/div, corresponding to 0 dBm input range of the oscilloscope, using the FFT with center frequency 950 MHz, span 4 GHz, RBW 100 kHz	–46 dBc (meas.)
Third order intercept point (TOI)	measured for two input tones with frequencies 2.436 GHz and 2.438 GHz and level 0 dBm at input sensitivity 160 mV/div, corresponding to 8 dBm input range of the oscilloscope, using the FFT with center frequency 2.437 GHz, span 10 MHz, RBW 30 kHz	23 dBm (meas.)

Waveform measurements

General features	measurement panels	up to 8 measurement panels; each panel may contain any number of automatic measurements of the same category
	gate	delimits the display region evaluated for automatic measurements
	reference levels	user-configurable vertical levels define support structures for automatic measurements
	statistics	displays maximum, minimum, mean, standard deviation, RMS and measurement count for each automatic measurement
	track	measurement results displayed as continuous trace that is time-correlated to the measurement source
	long-term analysis	history of selected measurements as trace against count index
	histogram	available for the main measurement of each measurement panel; automatic or manual selection of bin number and scale; counters for measurements under, within and over the histogram range
	limit check	measurements tested against user-defined margins and limits; pass or fail conditions may launch automatic response: acquisition stop, beep, print and save waveform

Measurement category	amplitude and time	amplitude, high, low, maximum, minimum, peak-to-peak, mean, RMS, sigma, overshoot, area, rise time, fall time, positive width, negative width, period, frequency, duty cycle, delay, phase, burst width, pulse count, positive switching, negative switching, cycle area, cycle mean, cycle RMS, cycle sigma, setup/hold time, setup/hold ratio, pulse train, slew rate rising, slew rate falling, DC voltmeter (requires Rohde & Schwarz active probe with R&S®ProbeMeter functionality)
	eye diagram	extinction ratio, eye height, eye width, eye top, eye base, crossing points, Q factor, S/N ratio, duty cycle distortion, eye rise time, eye fall time, eye bit rate, eye amplitude, jitter (peak-to-peak, 6-sigma, RMS)
	optical	optical average power, optical modulation amplitude
	spectrum	channel power, bandwidth, occupied bandwidth, harmonic search, total harmonic distortion THD in dB and % using power values, total harmonic distortion variants THD_a, THD_u and THD_r using voltage, overall voltage and overall voltage root means square, peak list (THD_a, THD_u and THD_r require R&S®RTO6-K37 option)
	jitter	cycle-to-cycle jitter, N-cycle jitter, cycle-to-cycle width, cycle-to-cycle duty cycle, time-interval error, data rate, unit interval, skew delay, skew phase; requires R&S®RTO6-K12 option
	EMC/ESD	first peak, second peak, I30, I60, time-to-value and level@delay; requires R&S®RTO6-K155 option
Cursors	setup	up to 4 cursor sets on screen, each set consisting of two horizontal and two vertical cursors
	target	acquired waveforms (input channels), math waveforms, reference waveforms, track waveforms, XY diagrams
	operating mode	vertical measurements, horizontal measurements or both; vertical cursors either set manually or locked to waveform
Histogram	source	acquired waveform (input channels), math waveform, reference waveform
	mode	vertical (for timing statistics), horizontal (for amplitude statistics)
	automatic measurements	waveform count, waveform samples, histogram samples, histogram peak, peak value, maximum, minimum, median, range, mean, sigma, mean ± 1, 2 and 3 sigma, marker ± probability

Mask testing

Test definition	number of masks	up to 8 simultaneously
	source	acquired waveforms (input channels), math waveforms
	fail condition	sample hit or waveform hit
	fail tolerance	minimum number of fail events for test fail in range from 0 to 4 000 000 000
	test rate	up to 600 000 waveforms/s
	action on error	acquisition stop, beep, print and save waveform
	save/load to file	test and mask settings (.xml format)
Mask definition with segments	number of independent segments	up to 8
	segment definition	array of points and connecting rule (upper, lower, inner) define segment region
	segment input	point and click on touchscreen, editable list
Mask definition with tolerance tube	input signal	acquired waveform
	definition of tolerance tube	horizontal width, vertical width, vertical stretch, vertical position
Mask definition with eye mask assistant (requires one of the following options: R&S®RTO6-K12/-K91/-K133/-K134)	primary mask shape	
	type	diamond, square, hexagon, octagon
	dimensions	main and secondary height, main and secondary width, depending on selected shape
	position	vertical offset, horizontal offset
	secondary mask shapes	
	locations	any combination of left, right, top, bottom
	position	horizontal and vertical offset with respect to center of primary mask shape
Serial standard masks	multiple predefined protocol masks	D-PHY, M-PHY, C-PHY, PCIe, USB, HDMI, JESD204C, ITU and Ethernet
Result statistics	category	completed acquisitions, remaining acquisitions, state, sample hits, mask hits, fail rate, test result (pass or fail)
Visualization options	waveform style	vectors, dots
	violation highlighting	hits (on/off), highlight persistence (50 ms to 50 s or infinite), waveform color (default: red)
	mask colors	configurable colors for mask without violation (default: translucent gray), mask with violation (default: translucent red), mask with contact (default: translucent pale red)

Waveform math

General features	number of math waveforms	up to 8
	number of reference waveforms	up to 4
	waveform arithmetic	user-selectable average or envelope of consecutive waveforms
Algebraic expressions	user may define complex mathematical expressions involving waveforms and measurement results	
	math functions	add, subtract, multiply, divide, absolute value, square, square root, integrate, differentiate, exp, $\log_{10}$, $\log_e$, $\log_2$, rescale, sin, cos, tan, arcsin, arccos, arctan, sinh, cosh, tanh, autocorrelation, crosscorrelation
	logical operators	not, and, nand, or, nor, xor, nxor
	relational operators	Boolean result of =, ≠, >, <, ≤, ≥
	frequency domain	spectral magnitude and phase, real and imaginary spectra, group delay
	digital filter	lowpass, highpass or user-defined filter (specified by up to 1 million FIR filter coefficients)
	special functions	CDR transform; requires R&S®RTO6-K12 option
Optimized math	operators	add, subtract, multiply, invert, absolute value, differentiate, $\log_{10}$, $\log_e$, $\log_2$, rescale, FIR, FFT magnitude

Spectrum analysis

General description	spectrum analysis allows signal analysis in the frequency domain.	
Spectrum	sources	channel 1, channel 2, channel 3, channel 4
	spectrum types	magnitude spectrum, phase spectrum
	setup parameters	center frequency, frequency span, automatic RBW, resolution bandwidth, gate position, gate width, vertical scale, vertical position, frame overlap
	scaling	
	magnitude spectrum	linear, dB, dBm, dBµV, dBmV, dBV, dBps, dBns, dBµs, dBms, dBs, dBHz, dBkHz, dBMHz, dBGHz, dBµA, dBmA, dBA
	phase spectrum	degrees, radians
	frequency range	DC to Nyquist frequency (1/2 sample rate, e.g. 10 GHz at 20 Gsample/s)
	frequency axis scaling	linear or logarithmic
	span	1 Hz to 10 GHz
	resolution bandwidth	≤ 1 Hz to 1 GHz
	window types	rectangular, Hamming, Hann, Blackman Harris, Gaussian, Flattop, Kaiser Bessel
	trace types	normal, envelope, average, RMS, min. hold, max. hold
	spectrum measurements	channel power, bandwidth, occupied bandwidth, various THD variants (total harmonic distortion), harmonic search, peak list (with user definable threshold)
	max. realtime waveform acquisition rate	> 1000 waveforms/s
	spectrogram	requires R&S®RTO6-K37 option

Search and mark function

General description	scans acquired waveforms for occurrence of a user-defined set of events and highlights each occurrence	
Basic setup	source	all physical input channels, math waveforms, reference waveforms
	search panels	up to 8, where each panel may manage multiple event searches
	search mode	manually triggered or continuous
	search conditions	
	supported events	edge, glitch, width, runt, window, timeout, interval, slew rate, data2clock, state
	event configuration	identical to corresponding trigger event
	event selection	single or multiple events on same source
Search oscilloscope	mode	current waveform, gated time interval
Result visualization	table	
	sort mode	horizontal position or vertical value
	max. result count	specifies max. table size
	zoom window	centered on highlighted event

Display characteristics

Diagram types	Yt, XY, spectrum, long-term measurement, spectrogram (spectrogram requires R&S®RTO6-K37 option)
Horizontal divisions	10
Vertical divisions	10
Display interface configuration	display area can be split up into separate diagram areas by dragging and dropping signal icons; each diagram area can hold any number of signals; diagram areas may be stacked on top of each other and later accessed via the dynamic tab menu
Signal icon	each active waveform is represented by a separate signal icon on the signal bar; the signal icon displays individual vertical and acquisition settings; a waveform can be minimized to signal icon to appears as a realtime preview in miniature; measurement results may also be minimized to a signal icon
Toolbar	quick access to 28 important tools; directly set most common parameters in a simple menu and access to more detailed parameters in main menu; user-defined selection of tools in toolbar
Upper menu	displays trigger, horizontal and acquisition settings; quick access to settings
Main menu	provides access to all instrument settings in compact menu
Axis label	X-axis ticks and Y-axis ticks labeled with tick value and physical unit
Diagram label	diagrams may be individually labeled with a descriptive user-defined name
Diagram layout	grid, crosshair, axis labels and diagram label may be switched on and off separately
Persistence	50 ms to 50 s, or infinite
Zoom	user-defined zoom window provides vertical and horizontal zoom; each diagram area supports multiple zoom windows; touchscreen interface simplifies resize and drag operations on zoom window
Signal colors	predefined or user-defined color tables for persistence display

Input and output

Front		
Channel inputs		BNC-compatible, for details see Vertical system
	probe interface	auto-detection of passive probes, Rohde&Schwarz active probe interface
Auxiliary output		SMA connector, for future use
Probe compensation output	signal shape	rectangle, V_{low} = 0 V, V_{high} = 1 V amplitude 1 V (V_{pp}) ± 5 %
	frequency	1 kHz ± 1 %
	impedance	nom. 50 Ω
Ground jack		connected to ground
USB interface		2 ports, type A plug, version 2.0

Rear		
External trigger input		BNC, for details see Trigger system
Trigger out		BNC, for details see Trigger system
USB interface		2 ports, type A plug and 1 port, type B plug, version 3.1 gen 1
LAN interface		RJ-45 connector, supports 10/100/1000BASE-T
External monitor interface		HDMI 2.0 and DisplayPort++ 1.3, output of oscilloscope display or extended desktop display
GPIB interface		see R&S®RTO6-B10 option
Reference input	connector	BNC female
	impedance	50 Ω (nom.)
	input frequency range	1 MHz to 20 MHz in steps of 1 MHz
	sensitivity at ≥ 2 MHz	≥ 0 dBm into 50 Ω
Reference output	connector	BNC female
	impedance	50 Ω (nom.)
	output signal with internal reference	10 MHz (specified in timebase accuracy), 7 dBm (nom.)
	output signal with external reference	none
Security slot		for standard Kensington style lock

General data

Display	type	15.6" LC TFT color display with capacitive touchscreen
	resolution	1920 × 1080 pixel (full HD)
Operating system		Windows 11
Hard disk drive		≥ 256 Gbyte removeable SSD

Temperature	operating	0 °C to +45 °C
	non-operating	–40 °C to +70 °C in line with MIL-PRF-28800F section 4.5.5.1.1.1 class 3
Humidity		+25° C/+40 °C at 85 % rel. humidity cyclic, in line with IEC 60068-2-30
		+30 °C/+40 °C/+45 °C at 95 %/75 %/45 %, in line with MIL-PRF-28800F section 4.5.5.1.1.2 class 3 for operation
Altitude	operating	up to 3000 m/9 843 ft above sea level
	non-operating	up to 4600 m/15 093 ft above sea level
Vibration	operating	sinusoidal: 5 Hz to 150 Hz, max. 1.8 g at 55 Hz; 0.5 g from 55 Hz to 150 Hz, in line with EN 60068-2-6
		5 Hz to 55 Hz, in line with MIL-PRF-28800F section 4.5.5.3.2 class 3
		random: 8 Hz to 500 Hz, acceleration 1.2 g (RMS), in line with EN 60068-2-64
		shock: 30 g functional shock, halfsine, duration 11 ms, in line with MIL-PRF-28800F section 4.5.5.4.1
	non-operating	random: 5 Hz to 500 Hz, acceleration 2.058 g (RMS), in line with MIL-PRF-28800F section 4.5.5.3.1 class 3
		shock: 40 g shock spectrum, in line with MIL-STD-810G, method no. 516.6, procedure I

EMC		
RF emission		in line with CISPR 11/EN 55011 group 1 class A (for a shielded test setup); instrument complies with EN 55011, EN 61326-1 and EN 61326-2-1 class A emission requirements and is suitable for use in industrial environments
Immunity		in line with IEC/EN 61326-1 table 2, immunity test requirements for industrial environment [6]

Certifications		VDE, $_{C}$CSA$_{US}$, CE, KC, UKCA, RCM
EU legislation	EU: in line with Data Act – Regulation (EU) 2023/2854	for details, see user documentation

Calibration interval		1 year

[6] Test criterion is displayed noise level within ±1 div for input sensitivity of 5 mV/div.

Power supply		
AC supply		100 V to 240 V at 50 Hz to 60 Hz and 400 Hz, max. 5.5 A to 2.3 A, in line with MIL-PRF 28800F section 3.5
Power consumption		max. 450 W
Safety		in line with IEC 61010-1/61010-2-030, EN 61010-1/61010-2-030, CAN/CSA-C22.2 No. 61010-1/ 61010-2-030, UL 61010-1/61010-2-030

Mechanical data		
Dimensions	W × H × D	450 mm × 315 mm × 204 mm (17.72 in × 12.40 in × 8.03 in)
Weight	without options, nominal	10.7 kg (23.59 lb)

Options

R&S®RTO6-B1 mixed signal option

Mixed signal option, additional 16 logic channels

Vertical system

Input channels		16 logic channels (D0 to D15)
Arrangement of input channels		arranged in two logic probes with 8 channels each, assignment of the logic probes to the channels (D0 to D7 or D8 to D15) is displayed on the probe
DC input resistance	at probe tips	100 kΩ ± 2 % (meas.)
Input capacitance		4 pF (meas.)
Maximum input frequency	signal with minimum input voltage swing and hysteresis setting: normal	400 MHz (meas.)
Maximum input voltage		±40 V (V_p); 32 V (RMS), derates to 7 V (RMS) with 20 dB/decade at frequencies above 25 MHz
Minimum input voltage swing		500 mV (V_{pp}) (meas.)
Resolution		1 bit
Threshold groups		D0 to D3, D4 to D7, D8 to D11 and D12 to D15
Threshold level	range	±8 V in steps of 25 mV
	predefined	CMOS 5.0 V, CMOS 3.3 V, CMOS 2.5 V, TTL, ECL, PECL, LVPECL
Threshold accuracy	threshold setting between ±4 V	±(100 mV + 3 % of threshold setting) (meas.)
Comparator hysteresis		normal, robust, maximum

Horizontal system

Channel deskew	range for each channel	±200 ns in steps of 200 ps
Channel-to-channel skew		< 500 ps (meas.)

Acquisition system

Sampling rate	max.	5 Gsample/s on each channel
Realtime waveform acquisition rate	max.	> 200 000 waveforms/s
Memory depth	at max. sampling rates	200 Mpoints for every channel
	at lower sampling rates	100 Mpoints for every channel
Decimation		pulses lost due to decimation are displayed
Minimum detectable pulse width		500 ps (meas.)

Trigger system

Holdoff range	time	100 ns to 10 s, fixed and random
	events	1 event to 2 000 000 000 events

Trigger modes		
Edge	triggers on specified slope (positive, negative or either) in the source signal	
	sources	any channel from D0 to D15 or any logical combination of D0 to D15
Width	triggers on positive or negative pulse of specified width in the source signal; width can be shorter, longer, equal, inside or outside the interval	
	sources	any channel from D0 to D15 or any logical combination of D0 to D15
	pulse width	200 ps to 10 s
Timeout	triggers when the source signal stays high, low or unchanged for a specified period of time	
	sources	any channel from D0 to D15 or any logical combination of D0 to D15
	timeout	200 ps to 10 s

Data2clock	triggers on setup time and hold time violations between a clock signal and a data signal; monitored time interval with a max. width of 200 ns and a position of max. ±1 µs relative to the clock edge	
	data signal	any subset of channels from D0 to D15 or any user-defined bus signal
	clock signal	any channel from D0 to D15
Pattern	triggers when the source goes true or stays true for a period of time shorter, longer, equal, inside or outside a specified range	
	sources	any logical combination of D0 to D15 or any user-defined bus signal
	pulse width	200 ps to 10 s
State	triggers on the slope (positive, negative or either) of the clock signal when data signal matches a user-defined logical state	
	data signal	any logical combination of D0 to D15 or any user-defined bus signal
	clock signal	any channel from D0 to D15
Serial pattern	triggers on a serial data pattern of up to 32 bit; pattern bits may be high (H), low (L) or don't care (X); clock edge slope may be positive, negative or either	
	data signal	any channel from D0 to D15 or any logical combination of D15 to D15
	clock signal	any channel from D0 to D15
	max. data rate	1 Gbps
Serial bus trigger	optional	see dedicated triggering and decoding options
	sources	any channel from D0 to D15

Waveform measurements

General features		measurement panels, gate, statistics, long-term analysis and limit check; see features of the base unit
Measurement sources		all channels from D0 to D15 or any logical combination of D0 to D15
Automatic measurements		positive pulse width, negative pulse width, period, frequency, burst width, delay, phase, positive duty cycle, negative duty cycle, positive pulse count, negative pulse count, rising edge count, falling edge count
Additional cursor function		display of decoded bus value at the cursor position

Display characteristics

Display of logical channels		selectable size and position on screen, diagram configuration by dragging and dropping signal icons
Bus decode	number of bus signals	4
	bus types	unclocked and clocked
	display types	decoded bus, logical signal, bus + logical signal, amplitude signal, amplitude + logical signal, tabulated list (decoded time interval selected with cursors)
	position and size	size and position on screen selectable
	data format of decoded bus	hex, unsigned integer, signed integer, fractional, binary
	data format of amplitude signal	unsigned integer, signed integer, fractional, binary offset
Channel activity display		independent of the oscilloscope acquisition, the state (stays low, stays high or toggles) of the channels from D0 to D15 is displayed in the signal icon

R&S®RTO6-B6 arbitrary waveform generator

Arbitrary function/waveform generator, 2 analog channels, 8 bit pattern generator

Analog channels

General		
Output channel		2 channels
Vertical resolution		14 bit
Operating modes		function generator, arbitrary waveform generator, modulation, frequency sweep

Function generator	output of predefined waveforms	
Sample rate		500 Msample/s
Waveforms	sine, square, ramp, DC, noise, pulse, cardinal sine (sinc), cardiac, Gaussian pulse, Lorentz, exponential rise, exponential fall	
Sine	frequency range	1 mHz to 100 MHz in steps of 1 mHz
	amplitude flatness (relative to 1 kHz)	
	f ≤ 100 kHz	≤ ±0.1 dB
	100 kHz < f ≤ 60 MHz	≤ ±0.3 dB
	60 MHz < f ≤ 100 MHz	≤ ±0.5 dB
	total harmonic distortion (THD at 1 V (V_{pp}) into 50 Ω)	
	f ≤ 100 kHz	≤ –70 dBc (= THD ≤ 0.032 %)
	100 kHz < f ≤ 15 MHz	≤ –55 dBc
	15 MHz < f ≤ 35 MHz	≤ –40 dBc
	35 MHz < f ≤ 100 MHz	≤ –30 dBc
	nonharmonic spurious (1 V (V_{pp}) into 50 Ω)	–65 dBc (meas.)
	phase noise (meas.)	
	f ≤ 25 MHz	≤ –105 dBc (1 Hz) at 1 kHz offset, ≤ –115 dBc (1 Hz) at 10 kHz offset, ≤ –125 dBc (1 Hz) at 100 kHz offset
	25 MHz < f ≤ 100 MHz	≤ –105 dBc (1 Hz) at 1 kHz offset, ≤ –110 dBc (1 Hz) at 10 kHz offset, ≤ –115 dBc (1 Hz) at 100 kHz offset
Square, pulse	frequency range	1 mHz to 30 MHz in steps of 1 mHz
	duty cycle (if pulse width limit is not exceeded)	0.01 % to 99.99 % in steps of 0.01 %
	duty cycle accuracy (meas.)	
	50 % duty cycle	≤ 0.001 % or ≤ 100 % · 150 ps · f whichever is larger f = frequency of square/ pulse signal
	any duty cycle	≤ 0.5 %
	pulse width	≥ 16.5 ns in steps of 0.1 ns
	rise/fall time	
	f ≤ 10 Hz	90 µs (meas.)
	10 Hz < f ≤ 30 MHz	9 ns (meas.)
	overshoot	≤ 2 %
	jitter (cycle-to-cycle)	≤ 40 ps (RMS) (meas.)
Ramp (triangle, sawtooth)	frequency range	1 mHz to 1 MHz in steps of 1 mHz
	linearity	≤ 0.1 % (meas.)
	variable symmetry	0 % to 100 % in steps of 0.1 %
DC	level range	
	into 50 Ω	± [3 V – (noise amplitude [V_{pp}] / 2)]
	into open circuit	± [6 V – (noise amplitude [V_{pp}] / 2)]
Noise	amplitude	
	DC	0 V to 6 V (V_{pp}) (into 50 Ω), 0 V to 12 V (V_{pp}) (into open circuit), 4 digits resolution
	all other waveforms	0 % to 100 % of AC signal amplitude, 1 % resolution
	bandwidth	≥ 100 MHz
Cardinal sine (sinc)	frequency range	1 mHz to 5 MHz
Cardiac	frequency range	1 mHz to 1 MHz
Gauss (Gaussian pulse)	frequency range	1 mHz to 25 MHz
Lorentz	frequency range	1 mHz to 10 MHz

Exponential rise/fall	frequency range	1 mHz to 1 MHz
Sine with 125 MHz	For 1000BASE-T1 compliance test measurements using the R&S®RTO6-K87 option and the R&S®RT-ZF6 frequency converter, the R&S®RTO6-B6 can be used to generate the 125 MHz signal for the transmitter distortion test.	

Arbitrary waveform generator	output of user-defined waveforms	
Waveform length		1 point to 40 Mpoints on each channel
Sample rate		1 sample/s to 250 Msample/s
Filter bandwidth		100 MHz
Modulation		
Sample rate		500 Msample/s
Modulation types		amplitude modulation (AM), frequency modulation (FM), frequency-shift key modulation (FSK), pulsewidth modulation (PWM)
Carrier waveform	AM, FM, FSK	sine
	PWM	square/pulse
AM	carrier frequency	1 mHz to 100 MHz
	modulation signals	sine, square, ramp (triangle, sawtooth)
	modulation frequency	1 mHz to 1 MHz
	modulation depth	0 % to 100 % in steps of 0.1 %
FM	carrier frequency	1 mHz to 100 MHz
	modulation signals	sine, square, ramp (triangle, sawtooth)
	modulation frequency	1 mHz to 1 MHz
	frequency deviation	1 mHz to 10 MHz
FSK	modulation signal	50 % duty cycle square wave
	range of frequency 1, frequency 2	1 mHz to 100 MHz
	hop rate	1 mHz to 1 MHz
PWM	carrier frequency	1 mHz to 30 MHz
	modulation signals	sine, square, ramp (triangle, sawtooth)
	modulation frequency	1 mHz to 1 MHz
	modulation depth	0 % to 99.99 % of the duty cycle, 0.01 % resolution

Frequency sweep	output of a sinusoidal waveform with the frequency changing linearly between the start frequency and the stop frequency within the sweep time	
	sample rate	500 Msample/s
	waveform	sine
	frequency range	1 mHz to 100 MHz
	direction	up (start frequency < stop frequency)
		down (start frequency > stop frequency)
	sweep time	1 ms to 500 s

Two-channel operation	operating modes	independent channels, coupled parameters, differential
	parameter coupling	none, frequency and/or amplitude
	relative phase	–180° to 180° in steps of 0.1°
	channel-to-channel skew	≤ 200 ps (meas.)
	channel-to-channel isolation (each channel with same output amplitude)	
	f ≤ 10 MHz	≥ 60 dB (meas.)
	10 MHz < f ≤ 100 MHz	≥ 40 dB (meas.)

Outputs		
Connectors		BNC female on the rear panel
Function		on/off, inverted
Output impedance		nom. 50 Ω
Overload protection		a short-circuit to ground is tolerated indefinitely, automatic shutoff in case of voltages ≥ +7 V or ≤ –7 V (meas.), automatic shutoff in case of overcurrent, max. –20 V to +20 V without damage (meas.), ESD protection
Amplitude range [7]	sine, square, ramp, pulse, exponential rise, exponential fall	
	into 50 Ω	
	frequency ≤ 50 MHz	10 mV to 6 V (V_{pp})
	frequency > 50 MHz to 100 MHz	10 mV to 4 V (V_{pp})
	into open circuit	
	frequency ≤ 50 MHz	20 mV to 12 V (V_{pp})
	frequency > 50 MHz to 100 MHz	20 mV to 8 V (V_{pp})
	cardinal sine (sinc), cardiac	
	into 50 Ω	10 mV to 3 V (V_{pp})
	into open circuit	20 mV to 6 V (V_{pp})
	Gauss (Gaussian pulse), Lorentz	
	into 50 Ω	10 mV to 2.5 V (V_{pp})
	into open circuit	20 mV to 5 V (V_{pp})
	arbitrary waveforms	
	into 50 Ω	
	sample rate ≤ 125 Msample/s	10 mV to 6 V (V_{pp})
	sample rate > 125 Msample/s	10 mV to 4 V (V_{pp})
	into open circuit	
	sample rate ≤ 125 Msample/s	20 mV to 12 V (V_{pp})
	sample rate > 125 Msample/s	20 mV to 8 V (V_{pp})
	resolution	1 mV
	accuracy	± [1% of control + 1 mV (V_{pp})] at 1 kHz
DC offset range	sine, square, ramp, pulse, exponential rise, exponential fall	
	into 50 Ω	± [3 V – (amplitude [V (V_{pp})] / 2)]
	into open circuit	± [6 V – (amplitude [V (V_{pp})] / 2)]
	cardinal sine (sinc), cardiac, Gauss (Gaussian pulse), Lorentz	
	into 50 Ω	±0.5 V
	into open circuit	±1 V
	resolution	1 mV
	accuracy	± (2 % of control + 2 mV)
Frequency accuracy		| Δf | ≤ [(timebase accuracy) × (nominal frequency) + 1 µHz] (timebase accuracy: see Horizontal system)

8 bit pattern generator

Function		output of user-defined patterns
Output channels		8 channels, coupled w.r.t. pattern length and data output rate
Pattern length		1 bit to 40 Mbit on each channel
Bit rate		1 bit/s to 40 Mbit/s

Outputs		
Connector		16-pin double row connector, 2.54 mm pitch, located on an adapter board, which is connected via a removable ribbon cable to the R&S®RTO6-B6
Output impedance		nom. 330 Ω
Overload protection	reverse input voltage without damage	–0.5 V to +6.5 V (meas.), ESD protection

[7] Amplitude is the sum of the AC amplitude and the noise amplitude.

Amplitude	low level output voltage (I = 100 µA)	
	output voltage	0 V + 0.15 V/– 0.02 V
	accuracy	≤ 0.15 V (meas.)
	high level output voltage	
	setting range	1.2 V to 5.0 V in steps of 0.1 V
	accuracy	≤ 0.05 V
Rise/fall time		8 ns (meas.)
Overshoot		≤ 5 % (meas.)

R&S®RTO6-B7 16 GHz differential pulse source

16 GHz differential pulse source with reference output

Output [8]

Output pulse		two complementary negative going square wave pulse train signals, single-ended or differential operation, fast transitionon rising and falling edge, adjustable amplitude and timing parameters, free-running or phase-locked to base unit
Outputs	single-ended operation	single-ended output (OutP)
		single-ended reference output (RefP)
	differential operation	differential output (OutP, OutN)
		differential reference output (RefP, RefN)
Output connectors		SMA female connectors
Reverse DC voltage		0 V
Output impedance	single-ended outputs	nom. 50 Ω
	both differential pairs	nom. 100 Ω
Return loss	≤ 10 GHz	> 15 dB (meas.)
	≤ 20 GHz	> 12 dB (meas.)

DC characteristics [8]

Output high level		0 V ± 10 mV
Output low level setting range		–200 mV to –50 mV, in steps of 10 mV
Output low level error	OutP	±2 % of setting ±15 mV
Output low level imbalance	between OutP and RefP, OutN, RefN	±1 dB (meas.)

Time domain characteristics [8]

Transition time	10 % to 90 %, rising and falling edge, calculated from 0.36/bandwidth	
	output low level	
	–120 mV to –50 mV	20 ps
	–200 mV to –130 mV	22 ps
Step response aberrations	for the first 100 ps after step transition	±10 % (meas.)
	for the first 1 ns after step transition	±4 % (meas.)
	until 100 ps before following step transition	±2 % (meas.)
Repetition rate	low frequency mode	5 Hz, 10 Hz, 20 Hz, 50 Hz, 100 Hz, 200 Hz, 500 Hz to 1 MHz
	high frequency mode, phase-locked to base unit	5 MHz, 10 MHz, 25 MHz, 50 MHz, 100 MHz, 250 MHz
	high frequency mode, free-running	5 MHz, 10 MHz, 25 MHz, 50 MHz
Positive duty cycle	measured at 50 % of transition	
	low frequency mode	10 % to 90 % in steps of 10 %
	high frequency mode	50 %
Duty cycle error	measured at 50 % of transition, at OutP and RefP outputs	
	low frequency mode	±2 % (meas.)
	high frequency mode	±0.1 % (meas.)

[8] All four outputs terminated with 50 Ω; all parameters are measured at all four single-ended outputs, unless noted.

Skew	measured at 50 % of transition, between OutP and OutN output	< 0.5 ps (meas.)
Clock accuracy	free-running	±100 ppm (meas.)
	phase-locked to base unit	see Timebase accuracy of base unit

Frequency domain characteristics [8]

Analog bandwidth (–3 dB)	output low level	
	–120 mV to –50 mV	> 18 GHz (meas.)
	–200 mV to –130 mV	> 16.5 GHz (meas.)
Spectral magnitude error to ideal step spectrum	≤ 5 GHz	+0.5 dB to –1 dB (meas.)
	≤ 12 GHz	+0.5 dB to –2 dB (meas.)
	≤ analog bandwidth	+0.0 dB to –3 dB (meas.)

General

Accessories	The R&S®RTO6-B7 contains an accessory bag with 2 SMA cables, 4 SMA terminations, 2 SMA(f) to SMA(f) adapters, 2 SMA shorts, 1 ESD wrist strap with grounding cord and 2 SMA(f) to BNC(m) adapters.

R&S®RTO6-B10 GPIB interface

Function		interface in line with IEC 625-2 (IEEE 488.2)
Command set		SCPI 1999.0
Connector		24-pin Amphenol female
Interface functions		SH1, AH1, T6, L4, SR1, RL1, PP1, DC1, DT1, C0

R&S®RTO6-B19 replacement solid state disk

Disk type		solid state disk
Disk size		nom. ≥ 240 Gbyte
Firmware		installed upon delivery

R&S®RTO6-K11 I/Q software interface

General	function	mixing, filtering, decimation and recording of RF or baseband signals as I/Q samples
	input signals	four real RF signals or two complex I/Q signals or two real RF signals and one complex I/Q signal
	mixer frequency	between 100 Hz and 5 GHz (or mixer deactivated)
	sampling rate of recorded I/Q samples	between 1 ksample/s and 10 Gsample/s
	digital filter bandwidth (flat frequency response)	4 % to 80 % of sampling rate
	sampling rate of recorded I/Q samples	between 1 ksample/s and 10 Gsample/s user-selectable
	recording length	
		recording length independent of sampling rate
	standard	max. 10 Mpoints with one or two input signals, max. 6 Mpoints with three or four input signals
	R&S®RTO6-B110 option	max. 40 Mpoints with one or two input signals, max. 24 Mpoints with three or four input signals
Trigger	mode	auto or normal
	operation	triggers on acquired signal after A/D conversion serial bus and MSO trigger not available
	additional modes	NFC-A, 106 kbps, SENSA_REQ; NFC-B, 106 kbps, SENSB_REQ; NFC-F, 202 kbps or 404 kbps, start of sequence (SoS) length: 48 bit or 96 bit
Display		magnitude of the downconverted signals

Amplitude flatness with RF signal input (meas.)	R&S®RTO6-B90 option	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 250 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 200 MHz	±0.12 dB	±0.30 dB
		≤ 300 MHz	±0.20 dB	±0.50 dB
		≤ 400 MHz	±0.25 dB	±0.70 dB
		≤ 500 MHz	±0.35 dB	±1.00 dB
	R&S®RTO6-B91 option	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 250 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 200 MHz	±0.10 dB	±0.15 dB
		≤ 500 MHz	±0.10 dB	±0.25 dB
		≤ 750 MHz	±0.15 dB	±0.40 dB
		≤ 1 GHz	±0.30 dB	±0.90 dB
	R&S®RTO6-B92 option	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.10 dB	±0.10 dB
		≤ 1 GHz	±0.17 dB	±0.35 dB
		≤ 1.5 GHz	±0.20 dB	±0.50 dB
		≤ 2 GHz	±0.35 dB	±1.00 dB
	R&S®RTO6-B93 option	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.10 dB	±0.10 dB
		≤ 1 GHz	±0.10 dB	±0.35 dB
		≤ 2 GHz	±0.10 dB	±0.35 dB
		≤ 3 GHz	±0.30 dB	±1.30 dB
	R&S®RTO6-B94 option	max. used center frequency	with I/Q bandwidth 100 MHz	with I/Q bandwidth 500 MHz
		≤ 100 MHz	±0.10 dB	
		≤ 500 MHz	±0.10 dB	±0.10 dB
		≤ 1 GHz	±0.10 dB	±0.10 dB
		≤ 2 GHz	±0.10 dB	±0.15 dB
		≤ 3 GHz	±0.12 dB	±0.30 dB
		≤ 4 GHz	±0.30 dB	±0.75 dB

R&S®RTO6-K12 jitter analysis

General description	The R&S®RTO6-K12 jitter analysis option extends the functionality of the standard R&S®RTO64 firmware with a suite of measurement, analysis and visualization tools for signal integrity analysis and jitter characterization.	
Waveform measurements	category	jitter
	measurement functions	cycle-to-cycle jitter, N-cycle jitter, cycle-to-cycle width, cycle-to-cycle duty cycle, time-interval error, data rate, unit interval, skew delay, skew phase; the standard time measurements period, frequency and setup/hold are also available in the jitter category for convenience
	track	measurement results displayed as continuous trace that is time-correlated to the measurement source; applicable to time measurements from categories “jitter” and “amplitude and time”; track trace may be used as source for cursor measurements, automatic measurements, math waveforms and reference waveforms
Waveform math	FFT on track	FFT spectrum of the track trace of measurement results
	CDR transform	recovers clock timing from source waveform with software CDR and generates synthetic clock waveform that is time-correlated to source

Software clock data recovery (CDR)	number of CDR instances	up to 2; independently configurable
	algorithm	phase-locked loop (PLL), constant frequency
	configuration	nominal bit rate, PLL order (first or second), PLL loop bandwidth, PLL damping factor, initial phase alignment, result selection during initial synchronization
Mask testing with eye mask assistant	primary mask shape	
	type	diamond, square, hexagon, octagon
	dimensions	main and secondary height, main and secondary width, depending on selected shape
	position	vertical offset, horizontal offset
	secondary mask shapes	
	locations	any combination of left, right, top, bottom
	position	horizontal and vertical offset with respect to center of primary mask shape

R&S®RTO6-K13 clock data recovery

General description	The R&S®RTO6-K13 realtime clock data recovery (CDR) option activates the hardware CDR circuitry integrated into the R&S®RTO64 oscilloscope. It provides realtime clock recovery for non-return-to-zero (NRZ) serial data up to 5.0 Gbps. The recovered clock may be used for triggering and jitter analysis.	
Hardware clock data recovery (CDR)	description	fully digital implementation of PLL-based clock data recovery
	sources	channel 1, channel 2, channel 3, channel 4
	configuration parameters	PLL order (first or second), nominal bit rate, loop bandwidth, relative bandwidth, damping factor, unit interval offset
	bit rate range	
	R&S®RTO6-B90, R&S®RTO6-B91, R&S®RTO6-B92, R&S®RTO6-B93 options	200 kbps to 2.5 Gbps
	R&S®RTO6-B94 option	200 kbps to 2.5 Gpbs standard, 400 kbps to 5.0 Gbps when operating at 20 Gsample/s realtime sampling rate [9]
	R&S®RTO6-B96 option	400 kbps to 5.0 Gbps standard, 200 kbps to 2.5 Gpbs when operating at 10 Gsample/s realtime sampling rate [10]
	relative bandwidth	1/500 to 1/3000 of the nominal bit rate
	damping factor	0.5 to 1.0; relevant for second order PLL only
	unit interval offset	0.0 to 1.0
Trigger modes	CDR	triggers on clock signal recovered from the trigger source signal; phase of the trigger instant user-selectable as fraction of bit period
	serial pattern	main trigger mode “serial pattern” supports the hardware CDR as additional clock source; sampling point user-selectable as fraction of bit period

[9] In general terms, the frontend of the R&S®RTO6-B94 option samples at 20 Gsample/s when: at most one channel from each pair {channel1, channel2} and {channel3, channel4} is active; and the user-selected sampling resolution in realtime sampling mode or interpolated time sampling mode is 50 ps or smaller.

[10] In general terms, the frontend of the R&S®RTO6-B96 option samples at 20 Gsample/s when at most one channel from each pair {channel1, channel2} and {channel3, channel4} is active, otherwise the sampling rate is 10 Gsample/s.

Jitter analysis	The data and clock timing information of the hardware CDR may be acquired in realtime concurrently to the input data waveform. Analysis of the realtime CDR timing information is possible by means of compatible measurement, analysis and visualization tools provided in the R&S®RTO6-K12 jitter analysis option. [11]	
	measurement functions	time-interval error (TIE), data rate, unit interval
	math functions	CDR transform interprets the acquired clock timing information and generates a synthetic clock waveform that is time-correlated to the input data waveform

R&S®RTO6-K21 USB 2.0 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde&Schwarz website. R&S®RTO6-K21 performs USB 2.0 compliance test measurements with R&S®ScopeSuite, including tests for USB 2.0 (high speed), USB 1.1 (full speed) and USB 1.0 (low speed) with the R&S®RTO. R&S®ScopeSuite supports the R&S®RT-ZF1 USB 2.0 compliance test fixture set, the Allion USB test fixture solutions and the USB-IF signal quality board device/host.

Supported USB 2.0 compliance tests		
USB device test	high speed	signal quality (EL_2, 4, 5, 6, 7); packet parameters (EL_21, 22, 25); chirp timing (EL_28, 29, 31); suspend/resume/reset timing (EL_27, 28, 38, 39, 40); test J/K, SE0_NAK (EL_8, 9); receiver sensitivity (EL_16, 17, 18)
	full speed and low speed	full speed signal quality; back voltage; inrush current
USB host test	high speed	signal quality (EL_2, 3, 6, 7); packet parameters (EL_21, 22, 23, 25, 55); chirp timing (EL_33, 34, 35); suspend/resume/reset timing (EL_39, 41); test J/K, SE0_NAK (EL_8, 9)
	full speed and low speed	low speed signal quality downstream; full speed signal quality downstream; drop; droop
USB hub test	high speed	signal quality upstream (EL_2, 4, 6, 7); signal quality downstream (EL_2, 3, 6, 7); jitter downstream (EL_47); packet parameters upstream (EL_21, 22, 25); hub receiver sensitivity upstream (EL_16, 17, 18); repeater downstream (EL_42, 43, 44, 45, 48); repeater upstream (EL_42, 43, 44, 45); chirp timing upstream (EL_28, 29, 31); suspend/resume/reset timing upstream (EL_27, 28, 38, 39, 40); test J/K, SE0_NAK upstream (EL_8, 9); test J/K, SE0_NAK downstream (EL_8, 9)
	full speed and low speed	low speed signal quality downstream; full speed signal quality upstream; full speed signal quality downstream; inrush current upstream; drop downstream; droop downstream; back voltage

[11] Realtime CDR timing information can be acquired when the frontend is operating at 10 Gsample/s realtime sampling rate.

R&S®RTO6-K22 Ethernet compliance test (10/100/1000BASE-T/EEE)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde&Schwarz website. R&S®RTO6-K22 performs Ethernet compliance test measurements with R&S®ScopeSuite, including tests for 10BASE-T, 100BASE-TX, 1000BASE-T and Energy Efficient Ethernet (EEE) with the R&S®RTO6. R&S®ScopeSuite supports the R&S®RT-ZF2 Ethernet compliance test fixture set as well as the R&S®RT-ZF4 and R&S®RT-ZF5 for.

Supported Ethernet compliance tests		
Standard reference		IEEE 802.3-2012
1000BASE-T	with/without disturber	with/without TX_CLK transmitter distortion (40.6.1.2.4)
		peak differential output voltage (40.6.1.2.1)
		maximum output droop (40.6.1.2.2)
		differential output templates (40.6.1.2.3)
	with TX_CLK	jitter master mode (40.6.1.2.5), jitter slave mode (40.6.1.2.5)
	without TX_CLK	jitter master mode (40.6.1.2.5)
	common	MDI return loss (40.8.3.1), common-mode output voltage (40.8.3.3)
100BASE-TX		amplitude domain tests (9.1.2.2, 9.1.3 and 9.1.4)
		rise and fall times (9.1.6)
		peak to peak duty cycle distortion (9.1.8)
		peak to peak transmitter jitter (9.1.9)
		active output interface template (annex J)
		transmitter return loss (9.1.5)
		receiver return loss (9.2.2)
10BASE-T	no TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		peak differential voltage (14.3.1.2.1)
		harmonic content (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	with TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		MAU template (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	common	transmitter return loss (14.3.1.2.2), receiver return loss (14.3.1.3.4)
		common-mode output voltage (14.3.1.2.5)

Supported EEE compliance tests		
Standard reference		IEEE 802.3-2012
1000BASE-T EEE (requires R&S®RT-ZF5)		quiet time (78.2)
		refresh time (master) (78.2)
		refresh time (slave) (78.2)
		wake state levels (40.6.1.2.7)
		transmitter timing jitter with TX_TCLK (master) (40.6.1.2.5)
		transmitter timing jitter with TX_TCLK (slave) (40.6.1.2.5)
		transmitter timing jitter without TX_TCLK (master) (40.6.1.2.5)
		transmitter timing jitter without TX_TCLK (master) (40.6.1.2.5)
100BASE-TX EEE (requires R&S®RT-ZF5)		sleep time (24.2.3.4 and 78.2)
		LPI quiet time (24.2.3.4 and 78.2)
		LPI refresh time (24.2.3.4 and 78.2)
		LPI transmitter timing jitter (24.2.3.4 and 78.2)
		transmit wake time (24.2.3.4 and 78.2)

10BASE-Te (requires R&S®RT-ZF4)	no TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		peak differential voltage (14.3.1.2.1)
		harmonic content (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	with TPM	link test pulse template (14.3.1.2.1)
		TP_IDL template (14.3.1.2.1)
		MAU template (14.3.1.2.1)
		output timing jitter (14.3.1.2.3)
	common	transmitter return loss (14.3.1.2.2), receiver return loss (14.3.1.3.4)
		common-mode output voltage (14.3.1.2.5)

R&S®RTO6-K23 Ethernet compliance test (2.5/5/10GBASE-T)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde&Schwarz website. R&S®RTO6-K23 performs Ethernet compliance test measurements with R&S®ScopeSuite, including tests for 2.5GBASE-T, 5GBASE-T and 10GBASE-T Ethernet with the R&S®RTO6. R&S®ScopeSuite supports the R&S®RT-ZF2 Ethernet compliance test fixture set. The option requires an R&S®RTO64 with a bandwidth ≥ 2 GHz.

Supported Ethernet compliance tests		
Standard reference		IEEE 802.3-2012 and IEEE P802.3bz
2.5G/5GBASE-T		maximum output droop (126.5.3.1)
		transmitter nonlinear distortion (126.5.3.2)
		transmitter timing jitter master mode and clock frequency (126.5.3.3 and 126.5.3.5)
		transmitter timing jitter slave mode (126.5.3.3)
		transmitter power spectral density and power level (126.5.3.4)
		MDI return loss (126.6.2.1)
10GBASE-T		maximum output droop (55.5.3.1)
		transmitter linearity (55.5.3.2)
		transmitter timing jitter master mode (55.5.3.3)
		transmitter timing jitter slave mode (55.5.3.3)
		transmitter power spectral density (55.5.3.4) [12]
		transmitter power level (55.5.3.4) [12]
		transmitter clock frequency (55.5.3.5)
		MDI return loss (55.8.2.1)

[12] Requires an oscilloscope model with a bandwidth higher than or equal 3 GHz.

R&S®RTO6-K24 Ethernet compliance test (100BASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTO6-K24 performs 100BASE-T1 compliance test measurements with R&S®ScopeSuite. R&S®ScopeSuite supports the R&S®RT-ZF2, R&S®RT-ZF7A and R&S®RT-ZF8 Ethernet compliance test fixtures. The chapters after the test cases refer to IEEE 802.3-2018 and OPEN Alliance ECU specification version 2.0.

Supported 100BASE-T1 compliance tests		
Standard reference		IEEE 802.3-2018
		OPEN Alliance ECU specification 2.0
100BASE-T1		transmitter output droop (96.5.4.1)
		transmitter distortion with and without disturber (96.5.4.2)
		transmitter timing jitter master mode (96.5.4.3)
		transmitter timing jitter slave mode (96.5.4.3)
		transmitter power spectral density (96.5.4.4)
		transmitter clock frequency (96.5.4.5)
		transmitter peak differential output (96.5.6)
		MDI return loss (96.7.1.3)
		MDI mode conversion Loss (96.8.2.2)
		MDI mode conversion Loss Adapter Verification (OABR_PMA_TX_06)
		MDI Common Mode Emission (OABR_PMA_TX_07)

R&S®RTO6-K26 MIPI D-PHY compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTO6-K26 performs D-PHY compliance test measurements with R&S®ScopeSuite.

Supported D-PHY compliance tests		
Standard reference		MIPI CTS for D-PHY V1.2
D-PHY	group 1 (7 tests): data lane LP-TX signaling requirements	data lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.1.1
		data lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.1.2
		data lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.1.3
		data lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.1.4
		data lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.1.5
		data lane LP-TX pulse width of exclusive-OR clock ($T_{LP\text{-}PULSE\text{-}TX}$) – 1.1.6
		data lane LP-TX period of exclusive-OR clock ($T_{LP\text{-}PER\text{-}TX}$) – 1.1.7
	group 2 (5 tests): clock lane LP-TX signaling requirements	clock lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.2.1
		clock lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.2.2
		clock lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.2.3
		clock lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.2.4
		clock lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.2.5
	group 3 (16 tests): data lane HS-TX signaling requirements	data lane HS entry: data lane T_{LPX} value – 1.3.1
		data lane HS entry: data lane $T_{HS\text{-}PREPARE}$ value – 1.3.2
		data lane HS entry: data lane $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ value – 1.3.3
		data lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.3.4
		data lane HS-TX differential voltage mismatch ΔV_{OD} – 1.3.5
		data lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.3.6
		data lane HS-TX static common-mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.3.7
		data lane HS-TX static common-mode voltage mismatch $\Delta V_{CMTX(1.0)}$ – 1.3.8
		data lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.3.9
		data lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.3.10
		data lane HS-TX from 20 % to 80 % rise time t_R – 1.3.11
		data lane HS-TX from 80 % to 20 % fall time t_F – 1.3.12
		data lane HS exit: $T_{HS\text{-}TRAIL}$ value – 1.3.13
		data lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.3.14
		data lane HS exit: T_{EOT} value – 1.3.15
		data lane HS exit: $T_{HS\text{-}EXIT}$ value – 1.3.16

D-PHY	group 4 (18 tests): clock lane HS-TX signaling requirements	clock lane HS entry: T_{LPX} value – 1.4.1
		clock lane HS entry: $T_{CLK-PREPARE}$ value – 1.4.2
		clock lane HS entry: $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ value – 1.4.3
		clock lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.4.4
		clock lane HS-TX differential voltage mismatch ΔV_{OD} – 1.4.5
		clock lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.4.6
		clock lane HS-TX static common-mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.4.7
		clock lane HS-TX static common-mode voltage mismatch $\Delta V_{CMTX(1,0)}$ – 1.4.8
		clock lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.4.9
		clock lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.4.10
		clock lane HS-TX from 20 % to 80 % rise time t_R – 1.4.11
		clock lane HS-TX from 80 % to 20 % fall time t_F – 1.4.12
		clock lane HS exit: $T_{CLK-TRAIL}$ value – 1.4.13
		clock lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.4.14
		clock lane HS exit: T_{EOT} value – 1.4.15
		clock lane HS exit: $T_{HS-EXIT}$ value – 1.4.16
		clock lane HS clock instantaneous: UI_{INST} value – 1.4.17
		clock lane HS clock delta UI: (ΔUI) value – 1.4.18
	group 5 (6 tests): HS-TX clock-to-data lane timing requirements	HS entry: $T_{CLK-PRE}$ value – 1.5.1
		HS exit: $T_{CLK-POST}$ value – 1.5.2
		HS clock rising edge alignment to first payload bit – 1.5.3
		data-to-clock skew ($T_{SKEW[TX]}$) – 1.5.4
		Initial HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.5
		Periodic HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.6

R&S®RTO6-K27 MIPI D-PHY 2.5 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde&Schwarz website. R&S®RTO-K27 performs D-PHY compliance test measurements with R&S®ScopeSuite. The numbers behind the test refer to the MIPI CTS for D-PHY V2.0, V2.1 and V2.5.

Supported D-PHY compliance tests		
D-PHY	group 1 (7 tests): data lane LP-TX signaling requirements	data lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.1.1
		data lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.1.2
		data lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.1.3
		data lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.1.4
		data lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.1.5
		data lane LP-TX pulse width of exclusive-OR clock ($T_{LP\text{-}PULSE\text{-}TX}$) – 1.1.6
		data lane LP-TX period of exclusive-OR clock ($T_{LP\text{-}PER\text{-}TX}$) – 1.1.7
	group 2 (5 tests): clock lane LP-TX signaling requirements	clock lane LP-TX Thevenin output high level voltage (V_{OH}) – 1.2.1
		clock lane LP-TX Thevenin output low level voltage (V_{OL}) – 1.2.2
		clock lane LP-TX from 15 % to 85 % rise time (T_{RLP}) – 1.2.3
		clock lane LP-TX from 85 % to 15 % fall time (T_{FLP}) – 1.2.4
		clock lane LP-TX slew rate versus C_{LOAD} ($\delta V/\delta t_{SR}$) – 1.2.5
	group 3 (16 tests): data lane HS-TX signaling requirements	data lane HS entry: data lane T_{LPX} value – 1.3.1
		data lane HS entry: data lane $T_{HS\text{-}PREPARE}$ value – 1.3.2
		data lane HS entry: data lane $T_{HS\text{-}PREPARE}$ + $T_{HS\text{-}ZERO}$ value – 1.3.3
		data lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.3.4
		data lane HS-TX differential voltage mismatch ΔV_{OD} – 1.3.5
		data lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.3.6
		data lane HS-TX static common mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.3.7
		data lane HS-TX static common mode voltage mismatch $\Delta V_{CMTX(1.0)}$ – 1.3.8
		data lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.3.9
		data lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.3.10
		data lane HS-TX from 20 % to 80 % rise time t_R – 1.3.11
		data lane HS-TX from 80 % to 20 % fall time t_F – 1.3.12
		data lane HS exit: $T_{HS\text{-}TRAIL}$ value – 1.3.13
		data lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.3.14
		data lane HS exit: T_{EOT} value – 1.3.15
		data lane HS exit: $T_{HS\text{-}EXIT}$ value – 1.3.16

D-PHY	group 4 (19 tests): clock lane HS-TX signaling requirements	clock lane HS entry: T_{LPX} value – 1.4.1
		clock lane HS entry: $T_{CLK-PREPARE}$ value – 1.4.2
		clock lane HS entry: $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ value – 1.4.3
		clock lane HS-TX differential voltages $V_{OD(0)}$ and $V_{OD(1)}$ – 1.4.4
		clock lane HS-TX differential voltage mismatch ΔV_{OD} – 1.4.5
		clock lane HS-TX single-ended output voltages $V_{OHHS(DP)}$ and $V_{OHHS(DN)}$ – 1.4.6
		clock lane HS-TX static common mode voltages $V_{CMTX(1)}$ and $V_{CMTX(0)}$ – 1.4.7
		clock lane HS-TX static common mode voltage mismatch $\Delta V_{CMTX(1, 0)}$ – 1.4.8
		clock lane HS-TX dynamic common-level variations from 50 MHz to 450 MHz $\Delta V_{CMTX(LF)}$ – 1.4.9
		clock lane HS-TX dynamic common-level variations above 450 MHz $\Delta V_{CMTX(HF)}$ – 1.4.10
		clock lane HS-TX from 20 % to 80 % rise time t_R – 1.4.11
		clock lane HS-TX from 80 % to 20 % fall time t_F – 1.4.12
		clock lane HS exit: $T_{CLK-TRAIL}$ value – 1.4.13
		clock lane HS exit: from 30 % to 85 % post-EoT rise time T_{REOT} – 1.4.14
		clock lane HS exit: T_{EOT} value – 1.4.15
		clock lane HS exit: $T_{HS-EXIT}$ value – 1.4.16
		clock lane HS clock instantaneous: UI_{INST} value – 1.4.17
		clock lane HS clock delta UI: (ΔUI) value – 1.4.18
		TX spread spectrum clocking (SSC) eequirements (1.4.19)
	group 5 (9 tests): HS-TX clock-to-data lane timing requirements	HS entry: $T_{CLK-PRE}$ value – 1.5.1
		HS exit: $T_{CLK-POST}$ value – 1.5.2
		HS clock rising edge alignment to first payload bit – 1.5.3
		data-to-clock skew ($T_{SKEW[TX]}$) – 1.5.4
		initial HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.5
		periodic HS skew calibration burst $T_{SKEWCAL-SYNC}$ $T_{SKEWCAL}$– 1.5.6
		Alternate calibration sequence $T_{ALTCAL-SYNC}$ and T_{ALTCAL} – 1.5.8
		preamble sequence $T_{PREAMBLE}$ and $T_{EXTSYNC}$ – 1.5.9
		clock and data lane TX HS-Idle $T_{HS-IDLE-POST}$, $T_{HS-IDLE-CLKHS0}$, $T_{HS-IDLE-PRE}$ – 1.5.10
	eye rest (3 tests)	clock lane HS clock delta UI (ΔUI) –1.4.18
		clock lane HS clock period jitter –1.4.20
		HS-TX data and clock eye diagram–1.5.7
Requirements		
Options	R&S®RTO6-K91 or R&S®RTO6-K136	DDR3 signal integrity and compliance or advanced eye analysis

R&S®RTO6-K31 power analysis

General description	The R&S®RTO6-K31 power analysis option extends the R&S®RTO64 firmware with measurement functionality focused on switched mode power supplies (SMPS) and DC/DC converters.	
Input	quality	evaluation of power quality at an AC input; measures real power, apparent power, reactive power, power factor and phase angle of power, frequency, crest factor, RMS of voltage and current
	harmonics	measures up to the 40th harmonic of the incoming line frequency; precompliance checking for IEC 61000-3-2 (A, B, C, D), RTCA DO-160, MIL-STD-1399, max. limit checks
	inrush current	measures peak inrush current; multiple measurement zones configurable with analysis of the post-inrush behavior
Switching/control loop	slew rate	The slope of current or voltage is measured at start and end of the switching cycle.
	modulation	measures modulation of switching frequency and duty cycle under steady state and start-up conditions
	dynamic on-resistance	measures resistance of the switching transistor(s) in active state
Power path	efficiency (only for 4 channel devices)	measures input and output power to calculate the efficiency of an SMPS
	loss	measures switching loss and conduction loss of a power device
	safe operating area (SOA)	checks violation of voltage and current limits in which a power device can operate without damage; current versus voltage view (linear or log); violation mask is user-defined and editable in linear and log-log views
	turn on/off	measures relationship between AC and DC current, when turning the SMPS off and on
Output	ripple	measures AC components of output voltage and current, AC RMS, frequency, duty cycles, min./max./peak-to-peak amplitude
	spectrum	FFT analysis of output, measurement of frequency peaks
	transient response	This measurement captures the device behavior between the event of load changes and stabilization; includes peak (voltage, time), settling time, rise time, overshoot and delay
Deskew	automated	By using the R&S®RT-ZF20 probe deskew and calibration test fixture and Rohde & Schwarz voltage and current probes, the skew between the voltage and current signal is compensated automatically.
Reporting	easy reporting: Click to save a measurement. Report generation using user-selected test results from historical and currently active tests. Put repeated and/or different measurements in one report.	

R&S®RTO6-K37 spectrogram

General description	The R&S®RTO6-K37 spectrum analysis allows advanced signal analysis in the frequency domain by visualization of the frequency spectrum versus time.	
Spectrogram	display characteristics	spectrogram display; a separate spectrogram can be created for each FFT display; each FFT segment of a captured acquisition is displayed in a separate spectrogram line
		support of logarithmic frequency x-axis
	number of spectrograms	up to 4
	signal colors	predefined or user-defined color tables for persistence display with the spectrogram
	timelines	in stop mode two separate timelines can be used to navigate through a spectrogram in time; for each timeline the relevant FFT segment is displayed in a diagram; the difference in acquisition time between the timelines is displayed
	measurements	THD_a, THD_u, THD_r

R&S®RTO6-K39 user-defined math

General description	The R&S®RTO6-K39 user-defined math option provides a Python interface to apply user functions defined by Python scripts to the waveform processing. The output can be visualized as a waveform math signal.

R&S®RTO6-K81 PCI Express 1.1/2.0 compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTO6-K81 performs PCIe 1.x/2.0 (up to 2.5GT/s) compliance test measurements with R&S®ScopeSuite. The option can only be used with an R&S®RTO6-B96 option.
The chapters after the category refer to PCI Express Base Specification Revision 1.1 and 2.1.

Supported PCIe compliance tests		
Standard reference		PCI Express Base Specification Revision 1.1 and 2.1
PCIe 1.1	signal quality (4.3.3)	mean unit interval
		data rate
		template tests
		min eye width
		median to max. jitter
		differential output voltage
	reference clock (1.32)	differential input high voltage
		differential input low voltage
		duty cycle
		average clock period
		rising edge rate
		falling edge rate
PCIe 2.0	signal quality (4.3.3)	mean unit interval
		data rate
		template tests
		min eye width
		median to max. jitter
		differential output voltage

R&S®RTO6-K87 Ethernet compliance test (1000BASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTO6-K87 performs 1000BASE-T1 compliance test measurements with R&S®ScopeSuite and R&S®RT-ZF7A and R&S®RT-ZF8 test fixtures. For the transmitter distortion test, the R&S®RT-ZF6 frequency converter is supported in combination with the R&S®RTO6-B6 AWG (running in 125 MHz mode). The option requires an R&S®RTO64 with a bandwidth ≥ 2 GHz.

Supported 1000BASE-T1 compliance tests	
Standard reference	IEEE 802.3-2018 (OPEN Alliance ECU specification supported, where applicable)
1000BASE-T1	97.5.3.3 transmitter timing jitter master mode
	97.5.3.3 transmitter timing jitter slave mode
	97.5.3.3 transmitter timing MDI jitter
	97.5.3.6 transmitter clock frequency
	97.5.3.2 transmitter distortion
	97.5.3.4 transmitter power spectral density (PSD)
	97.5.3.4 transmitter power level
	97.5.3.5 transmitter peak differential output
	97.5.3.1 maximum output droop
	97.7.2.1 MDI return loss
	97.7.2.2 MDI mode conversion loss
	MDI adapter verification

R&S®RTO6-K88 Ethernet compliance test (MGBASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTO6-K88 performs MGBASE-T1 compliance test measurements with R&S®ScopeSuite. R&S®ScopeSuite supports R&S®RT-ZF7A and R&S®RT-ZF8 test fixtures.
The chapters in front of the test cases refer to IEEE P802.3ch.

Supported MGBASE-T1 compliance tests	
MGBASE-T1 (2.5/5/10G)	149.5.2.1 maximum output droop
	149.5.2.2 transmitter linearity
	149.5.2.3 transmitter timing jitter master
	149.5.2.3 transmitter timing jitter slave
	149.5.2.3.1 transmit MDI random jitter in master mode
	149.5.2.3.2 transmit MDI deterministic jitter in master mode
	149.5.2.4 transmitter power spectral density (PSD) and power level
	149.5.2.5 transmitter peak differential output
	149.5.2.6 transmitter clock frequency
	149.8.2.1 MDI return loss

R&S®RTO6-K89 Ethernet compliance test (10BASE-T1)

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTO6-K89 performs 10BASE-T1 compliance test measurements with R&S®ScopeSuite. R&S®ScopeSuite supports the R&S®RT-ZF7A and R&S®RT-ZF8 test fixtures.

Supported 10BASE-T1 compliance tests	
Standard reference	IEEE P802.3cg
10BASE-T1S	147.5.4.1 transmitter output voltage
	147.5.4.3 transmitter timing jitter
	147.5.4.2 transmitter output droop
	147.5.4.4 transmitter power spectral density (PSD)
	147.7.2 MDI return loss
	147.7.3 MDI mode conversion
10BASE-T1L	146.5.4.1 transmitter output voltage
	146.5.4.3 transmitter timing jitter
	146.5.4.5 transmitter clock frequency
	146.5.4.4 transmitter power spectral density (PSD) and power level
	146.8.3 MDI return loss
	146.8.4 MDI mode conversion

R&S®RTO6-K91 DDR3/DDR3L/LPDDR3 signal integrity debug and compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde & Schwarz website. R&S®RTO6-K91 performs DDR3, DDR3L and LPDDR3 compliance test measurements with R&S®ScopeSuite. Furthermore, it enables the DDR3 decode capability to separate read and write bursts as well as the eye analysis function for mask testing on the oscilloscope.

Supported DDR3 compliance tests		
Standard reference	DDR3	JESD79-3F
	DDR3L	JESD79-3-1A.01
	LPDDR3	JEDS209-3C
Timing tests	clock timing (12.1)	tCK(avg) (12.1.1)
		tCK(abs) (12.1.2)
		tCL(avg) (12.1.3)
		tCH(avg) (12.1.3)
		tJIT(per) (12.1.4)
		tJIT(duty) (12.1.4)
		tJIT(cc) (12.1.5)
		tERR(nper) (12.1.6)
	data timing (4.13.2, 13.4, 13.6)	tDS(base) (13.6)
		tDH(base) (13.6)
		tDS(derate) (13.6)
		tDH(derate) (13.6)
		tHZ (4.13.2)
		tLZ (4.13.2)
		tDIPW (13.4 note 28)
		tDQSQ (4.13.2)
		tQH (4.13.2)
	strobe timing (4.13, 4.14, 8.3.1)	tDQSCK (4.13.2)
		tLZ (4.13.2)
		tHZ (4.13.2)
		tRPRE (4.13.2)
		tRPST (4.13.2)
		tQSH (4.13.2)
		tQSL (4.13.2)
		tDQSS (4.14.2)
		tDQSH (4.14.2)
		tDQSL (4.14.2)
		tDSS (4.14.2)
		tDSH (4.14.2)
		tWPST (4.14.2)
		tWPRE (4.14.2)
		tDVAC (strobe) (8.3.1)
		tDVAC (clock) (8.3.1)
	command timing (13.5)	tIS (13.5)
		tIS (derated) (13.5)
		tIH (13.5)
		tIH (derated) (13.5)
		tIPW (13.5)
		tVAC (CA) (13.5)
	address timing (13.5) DDR3 and DDR3L	tIS (13.5)
		tIS (derated) (13.5)
		tIH (13.5)
		tIH (derated) (13.5)
		tIPW (13.5)
		tVAC (CA) (13.5)
	address timing (4.2) LPDDR3	tISCA (4.2)
		tIHCA (4.2)
		tIPWCA (4.2)
		tVAC (CA) (13.5)
	chip select timing (13.5) DDR3 and DDR3L	tIS (13.5)
		tIS (derated) (13.5)
		tIH (13.5)
		tIH (derated) (13.5)
		tIPW (13.5)

	chip select timing (4.2) LPDDR3	tISCS (4.2)
		tIHCS (4.2)
		tIPWCS (4.2)
		tVAC(CS) (11.5)
Electrical tests single-ended measurements	input slew rate for ADD and CMD DDR3 and DDR3L (8.5, 13.5) LPDDR3 (7.6, 11.5)	SR(tIS) rising
		SR(tIS) falling
		SR(tIH) rising
		SR(tIH) falling
	input slewrate for DQ and DM DDR3 and DDR3L (8.5, 13.6) LPDDR3 (7.6, 11.6)	SR(tIS) rising
		SR(tIS) falling
		SR(tIH) rising
		SR(tIH) falling
	AC and DC input levels for ADD and CMD DDR3 (8.1.1) DDR3L (3.1) LPDDR3 (7.1.1)	VIH (AC)
		VIL (AC)
		VIH (DC)
		VIL (DC)
	AC and DC input levels for DQ and DM (8.1.2)	VIH (AC)
		VIL (AC)
		VIH (DC)
		VIL (DC)
	AC input levels for CK and DQS (8.3.3)	VSEH (AC)
		VSEL (AC)
	output slew rate for DQ (9.3)	SRQse rising
		SRQse falling
	AC and DC output levels for DQ (9.2)	VOH(AC)
		VOL(AC)
		VOH(DC)
		VOL(DC)
	AC overshoot and undershoot for ADD and CMD (9.6.1)	overshoot amplitude
		overshoot area
		undershoot amplitude
		undershoot area
	AC overshoot and undershoot for CK, DQ, DQS and DM (9.6.2)	overshoot amplitude
		overshoot area
		undershoot amplitude
		undershoot area
Electrical tests differential measurements	AC input levels for CK and DQS (8.3)	VIHdiff (AC)
		VILdiff (AC)
	AC differential cross point voltage for CK and DQS (8.4)	VIX (AC)
	differential output slew rate for DQS (9.4)	SRQdiff rising
		SRQdiff falling
	differential AC output levels for DQS (9.2)	VOHdiff(AC)
		VOLdiff(AC)
Debug	trigger write cycle	configures the oscilloscope to trigger on a write cycle
	trigger read cycle	configures the oscilloscope to trigger on a read cycle
DDR3 decoding		
Protocol configuration	signal type	DQ, DQS
	bit rate	adjustable
	threshold setup	manual threshold/hysteresis configuration
	source	analog channels
Decode	display type	decoded bus, tabulated list, details
	color coding	read frame, write frame
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, words
Search	search event setup	frame content, error
	frame content	data; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	error	length, frame incomplete

DDR3 eye diagram		
General description	The DDR3 eye diagram allows the user to generate eye diagrams from long multi-period acquisitions of clock signals and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the development advanced analysis, measurement, mask test and navigation functions.	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate
Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than, in range, out of range; relative to selected reference level
Filter	DDR3 protocol	
	frame type	any, read frame, write frame
	error	length
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bit and up to 5 suffix bit with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item

R&S®RTO6-K92 eMMC compliance test

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde&Schwarz website. R&S®RTO6-K92 performs eMMC (HS200, HS400) compliance test measurements with R&S®ScopeSuite.

Supported eMMC compliance tests		
Standard reference		JESD84-B50
HS200	CLK (10.5.2, 10.8.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (t_{Period}, rise time, fall time, duty cycle)
	CMD push pull (10.5.2, 10.8.1)	bus signal levels tests (VIH, VIL, VOH, VOL)
		interface timing tests (setup time, hold time)
	CMD open drain (10.5.1)	bus signal levels tests (VOH, VOL)
	DAT data write (10.5.2, 10.8.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (setup time, hold time)
	DAT data read (10.5.2, 10.8.1)	bus signal levels tests (VOH, VOL)
HS400	CLK (10.5.2, 10.10.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (t_{Period}, slew rate, duty cycle distortion, minimum pulse width)
	CMD push pull (10.5.2, 10.10.1)	bus signal levels tests (VIH, VIL, VOH, VOL)
		interface timing tests (setup time, hold time)
	CMD open drain (10.5.1)	bus signal levels tests (VOH, VOL)
	DAT data write (10.5.2, 10.10.1)	bus signal levels tests (VIH, VIL)
		interface timing tests (setup time, hold time, slew rate)
	DAT data read (10.5.2, 10.10.2)	bus signal levels tests (VOH, VOL)
		interface timing tests (output skew, output hold skew, slew rate)
	data strobe for data read (10.5.2, 10.10.1)	bus signal levels tests (VOH, VOL)
		interface timing tests (t_{Period}, slew rate, duty cycle distortion, minimum pulse width)

R&S®RTO6-K99 R&S®ScopeSuite automation

The option is used in combination with the free-of-charge R&S®ScopeSuite PC software, which can be downloaded from the Rohde&Schwarz website. It requires matching compliance test options (see below). R&S®RTO6-K99 makes it possible to automate the supported compliance options remotely. After remote execution of a test case the user can collect the results to process them in a proprietary software to create own reports.

Remote API to execute test cases of R&S®ScopeSuite		
API language		C#
Supported options	R&S®RTO6-K22	100BASE-TX, 1000BASE-T
	R&S®RTO6-K24	100BASE-T1
	R&S®RTO6-K87	1000BASE-T1
	R&S®RTO6-K91	DDR3, DDR3L, LPDDR3

R&S®RTO6-K121 deembedding base option

General description	The R&S®RTO6-K121 deembedding base option allows waveform correction based on S-parameters of the involved measurement blocks. The R&S®RTO6-K121 option is available for R&S®RTO6-B92, R&S®RTO6-B93, R&S®RTO6-B94 and R&S®RTO6-B96 options only.	
Source		channel 1, channel 2, channel 3, channel 4,
Signal types		single-ended signals
		differential signals based on two separate cables by using two channels
		full differential signals based on differential probes
S-parameter files		s2p-files and s4p-files
Types of blocks		cables, connectors, fixtures and customer defined blocks
Maximum number of blocks		10

Proven cable/proven probe

General description	The proven probe/proven cable is a part of the R&S®RTO6-K121 deembedding base option. This function enables the user to determine the correction parameters of a cable or a modified probe based on the differential pulse source R&S®RTO6-B7.	
Mode		proven cable proven probe (Rohde & Schwarz probes, user defined)
Configurations	proven cable	single ended
	proven probe	single ended, differential
Correction method	cable, user-defined probe	transmission (magnitude and phase)
	Rohde & Schwarz probe	transmission (magnitude and phase)
Maximal group delay of DUT		20 ns
Maximal length of cables (setup)		3 m
Source		step with amplitude of –200 mV

R&S®RTO6-K126 embedding and equalization option

General description	The R&S®RTO6-K126 option consists of equalization (used to compensate for transmission losses and to re-open the data eye) and embedding (provides the users with the capability to emulate additional signal traces (e.g.: longer cables)).	
Lane configuration	number of lane instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels
	vertical settings	scale, offset, position
Embedding	signal types	single ended, full differential
	S-parameter files	s2p-files and s4p-files
	block types	cables, adapters, fixtures, proven cable, and customer defined blocks
	maximum number of blocks	5
Equalization	transmission feed forward equalizer (TxFFE)	
	presets	predefined presets (dependent on the selected serial standard)
	filter taps	up to 4 taps
	continuous time linear equalizer (CTLE)	
	presets	predefined presets (dependent on the selected serial standard)
	DC gain	desired DC gain in dB
	zero frequencies	up to 6 zeros
	pole frequencies	up to 6 poles
	feed forward equalizer (FFE)	
	filter taps	up to 40 taps
	taps per symbol	track data rate, manual

	decision feedback equalizer (DFE)	
	timing reference	clock, CDR
	clock source	analog channels, differential channels, math channels, reference channels
	CDR	
	type	software
	sampling time	0.0 to 1.0 UI
	filter taps	up to 5 taps
	gain	desired gain [scalar]
	FFE and DFE training	
	mode	main source, reference waveform
	filter	FFE, FFE and DFE
	FFE	
	taps	up to 40 taps
	precursor taps	up to 39 taps
	taps per symbol	track data rate, manual
	DFE	
	taps	up to 5 taps
	tap lower limit	–1.0 to 1.0
	tap upper limit	–1.0 to 1.0
	normalize gain	filter taps will be trained to achieve a normalized gain

R&S®RTO6-K130 TDR/TDT analysis

Time domain reflexion/time domain transmission analysis option		
General description	The R&S®RTO6-K130 TDR/TDT option is a measurement technique used to determine the characteristics of electrical lines by observing reflected and/or transmitted waveforms. Together, they provide a powerful means of analyzing electrical transmission media. The R&S®RTO6-K130 option is available for R&S®RTO6-B92, R&S®RTO6-B93, R&S®RTO6-B94 and R&S®RTO6-B96 options only.	
Mode		TDR, TDT, TDR/TDT
Configuration		single ended
Signals		impedance/reflection coefficient
Domain		time/distance
Bandwidth	TDR and/or TDT, single ended	
	R&S®RTO6-B92	2 GHz
	R&S®RTO6-B93	3 GHz
	R&S®RTO6-B94	4 GHz
	R&S®RTO6-B96	6 GHz
Step amplitude		200 mV
Repetition rate		50 Hz to 500 kHz (depends on horizontal scale)
Length of cable	max.	15 ns (~ 3.2 m at $\varepsilon_r = 2$)
	min.	2 ns (~ 0.4 m at $\varepsilon_r = 2$)
Electrical length of short	range, adjustable by user	0 ns to 2 ns
Reference impedance	single ended	50 Ω

R&S®RTO6-K133 advanced jitter analysis

General description	The R&S®RTO6-K133 option provides advanced jitter measurements and enables jitter separation. R&S®RTO6-K133 option includes R&S®RTO6-K12 option.	
Jitter separation	total jitter (TJ), deterministic jitter (DJ), data dependent jitter (DDJ), periodic jitter (PJ), data dependent jitter plus periodic jitter (DDJ+PJ), random jitter (RJ), (other) bounded uncorrelated jitter ((O)BUJ), random jitter plus (other) bounded uncorrelated jitter (RJ+(O)BUJ)	
Accepted input signals	clock signals or data signals (NRZ)	
Reference clock	internal clock recovery (PLL first or second order, constant clock or feed forward) or explicit clock signal	
Basic measurements	symbol rate, symbol duration, event count	
Jitter measurements	total jitter at bit error rate (TJ@BER)	value in seconds or unit interval BER value selectable between 10^{-32} and 10^{-1}
	deterministic jitter (DJ, dual-dirac)	value in seconds or unit interval
	duty cycle distortion (DCD)	value in seconds or unit interval
	inter symbol interference (ISI)	value in seconds or unit interval
	total jitter (TJ) corresponds to time interval error (TIE)	peak-to-peak value and RMS value in seconds or unit interval
	deterministic jitter (DJ)	peak-to-peak value and RMS value in seconds or unit interval
	data dependent jitter (DDJ)	peak-to-peak value and RMS value in seconds or unit interval
	periodic jitter (PJ)	peak-to-peak value and RMS value in seconds or unit interval
	data dependent jitter plus periodic jitter (DDJ+PJ)	peak-to-peak value and RMS value in seconds or unit interval
	periodic jitter components	amplitude, frequency, direction (vertical or horizontal)
	random jitter (RJ)	RMS value in seconds or unit interval
	(other) bounded uncorrelated jitter ((O)BUJ),	peak-to-peak value and RMS value in seconds or unit interval
	(other) bounded uncorrelated jitter ((O)BUJ, dual-dirac),	value in seconds or unit interval
	random jitter plus (other) bounded uncorrelated jitter (RJ+(O)BUJ)	peak-to-peak value and RMS value in seconds or unit interval
Statistics	max. and min. values for each jitter measurement type	
Jitter result plots	histogram (rising edges only)	TJ, DJ, DDJ, PJ, RJ+OBUJ
	histogram (falling edges only)	TJ, DJ, DDJ, PJ, RJ+OBUJ
	histogram (both edges)	TJ, DJ, DDJ, PJ, RJ+OBUJ
	TIE track	TJ, DDJ, PJ, RJ+OBUJ
	power spectral density (PSD)	TJ, DDJ, PJ, RJ+OBUJ
Additional result plots	step response	
	bathtub	PJ and (O)BUJ removable from noise bathtub
	synthetic eye diagram	DD only, DD+P(h), DD+P(v), DD+P
	reconstructed signal	composite signal of calculated jitter and noise measurement values
	error signal	difference signal of original input signal and reconstructed signal

R&S®RTO6-K134 advanced jitter and noise analysis

General description	The R&S®RTO6-K134 option provides advanced jitter and noise measurements and separation. R&S®RTO6-K134 option includes advanced jitter analysis R&S®RTO6-K133 option and basic jitter analysis R&S®RTO6-K12 option.	
Noise separation	total noise (TN), deterministic noise (DN), data dependent noise (DDN), periodic noise (PN), data dependent noise plus periodic noise (DDN+PN), random noise (RN), (other) bounded uncorrelated noise ((OBUN), random noise plus other (other) bounded uncorrelated noise (RN+(O)BUN)	
Accepted input signals	clock signals or data signals (NRZ)	
Reference clock	internal clock recovery (PLL first or second order, constant clock or feed forward) or explicit clock signal	
Basic measurements	symbol rate, symbol duration, event count	
Noise measurements	eye height at bit error rate (EN@BER)	absolute or relative, BER value selectable between 10^{-32} and 10^{-1}
	level distortion (LD)	absolute or relative value
	inter symbol interference noise (ISIN)	absolute or relative value
	total noise (TN)	peak-to-peak value and RMS value, absolute or relative
	deterministic noise (DN)	peak-to-peak value and RMS value, absolute or relative
	data dependent noise (DDN)	peak-to-peak value and RMS value, absolute or relative
	periodic noise (PN)	peak-to-peak value and RMS value, absolute or relative
	data dependent noise plus periodic noise (DDN+PN)	peak-to-peak value and RMS value, absolute or relative
	periodic noise components	amplitude, frequency, direction (vertical or horizontal)
	random noise (RN)	RMS value, absolute or relative
	(other) bounded uncorrelated noise ((O)BUN)	peak-to-peak value and RMS value, absolute or relative
	(other) bounded uncorrelated noise ((O)BUN, dual-dirac)	absolute or relative value
	random noise plus (other) bounded uncorrelated noise (RJ+(O)BUN)	peak-to-peak value and RMS value, absolute or relative
Statistics	max. and min. values for each noise measurement type	
Noise result plots	histogram (level 0)	TN, DN, DDN, PN, RN+OBUN
	histogram (level 1)	TN, DN, DDN, PN, RN+OBUN
	histogram (both levels)	TN, DN, DDN, PN, RN+OBUN
	TIE track	TN, DDN, PN, RN+OBUN
	power spectral density (PSD)	TN, DDN, PN, RN+OBUN
Additional result plots	step responses	
	noise bathtub	PN and (O)BUN removable from noise bathtub
	synthetic eye diagram	DD only, DD+P(h), DD+P(v), DD+P
	reconstructed signal	composite signal of calculated jitter and noise measurement values
	error signal	difference signal of original input signal and reconstructed signal

R&S®RTO6-K135 PAM-N analysis

General description	The R&S®RTO6-K135 option extends R&S®RTO6-K133 advanced jitter analysis, R&S®RTO6-K134 advanced jitter and noise analysis and R&S®RTO6-K136 advanced eye analysis for pulse amplitude modulated (PAM) signals up to PAM order 8.	
Signal configuration	number of PAM-N input signal sources	up to 8; independently configurable in technology, serial standard, PAM order and symbol rate
	main sources	analog channels, differential channels, math channels and reference channels
Timing references	advanced jitter and noise analysis	
	explicit clock	NRZ signal
	internal software clock recovery	up to 5 GBaud (depending on device bandwidth)
	advanced eye analysis	
	explicit clock	NRZ signal
	internal software clock recovery	up to 5 GBaud (depending on device bandwidth)
Measurements	advanced jitter and noise analysis	
	basic	see R&S®RTO6-K133/-K134
	jitter	see R&S®RTO6-K133 incl. all possible level transitions up to PAM level 8
	noise	see R&S®RTO6-K134 incl. all possible signal levels up to PAM level 8
	statistics	maximum and minimum for each basic, jitter and noise measurement
	presets	all selected components with explicit level height, one selected component with same level heights or one selected component with same base level
	advanced eye analysis	
	eye	amplitude, rise time, fall time, slew rate rising, slew rate falling and signal levels
	statistics	maximum, minimum, mean, standard deviation, RMS and measurement count for each eye measurement
	presets	depending on additional filters whole, specific or selected eye
Result plots	advanced jitter and noise analysis	
	histogram	see R&S®RTO6-K133/-K134 incl. all possible level transitions up to PAM level 8
	track	see R&S®RTO6-K133/-K134 incl. all possible signal levels up to PAM level 8
	advanced eye analysis	
	eye diagram	eye with N-1 eye openings
Additional result plots	advanced jitter and noise analysis	
	jitter bathtub	see R&S®RTO6-K133
	noise bathtub	see R&S®RTO6-K134 incl. N-1 valleys
Additional filters	advanced eye analysis	
	whole eye	N-1 eye openings with all level transitions
	specific eye	one explicit eye opening with all involved level transitions
	selected eye	an explicit eye opening with only its own level transition

R&S®RTO6-K136 advanced eye analysis

General description	The advanced eye analysis allows the user to generate eye diagrams from long multi-period acquisitions of clock signals, and serial data signals. It allows the fine control of the signal content that contributes to the eye diagram and enables the advanced analysis, measurement, mask test and navigation functions. The supported data rate depends on the available input clocks (e.g. SW CDR or clock signal).	
General configuration	number of eye diagram instances	up to 4; independently configurable
	main source	analog channels, differential channels, math channels, reference channels, track channels
	timing reference source	analog channels, differential channels, math channels, reference channels, track channels
	horizontal settings	range, position; expressed in absolute time or relative to user-defined bit rate
	vertical settings	scale, offset, position
Display	persistence	50 ms to 50 s, or infinite
	trace colors	predefined or user-defined color tables
	eye stripe	displays position of eye diagram slices and masks violations time-correlated to the main source waveform; always enabled, for mask tests only, disabled
Qualification	gate	
	position	start, stop; absolute time or relative to display in percent
	coupling	none, cursor, zoom
	signal	
	source	analog channels, math channels, reference channels
	condition	greater than, less than, in range, out of range; relative to selected reference levels
Filter	DDR3/DDR4 protocol	
	frame type	any, read frame, non-consecutive read frame, write frame, non-consecutive write frame
	error	length
	bit sequence	
	mode	all, level transition, constant level, bit pattern
	bit pattern setup	up to 8 prefix bits and up to 5 suffix bits with respect to central eye diagram bit
Mask testing	mask test results	
	counters	acquisitions, slices, sample hits, slice hits, fail rate
	violation details	number and position of mask violation, expressed as time instant and slice index
	navigation and zoom	use zoom coupling to navigate to violation upon clicking the corresponding table item

R&S®RTO6-K155 EMC/ESD analysis

General description	The R&S®RTO6-K155 EMC/ESD option extends the functionality of the standard R&S®RTO64 firmware with a suite of measurement, analysis and visualization tools for electromagnetic compliance (EMC)/electrostatic discharge (ESD) analysis and characterization.	
Waveform measurements	category	EMC/ESD
	measurement functions	first peak, second peak, I30, I60, time-to-value and level@delay; the standard time measurements rise/fall time are also available in this category for convenience

R&S®RTO6-K500 bus analysis

General description	The R&S®RTO6-K500 bus analysis option adds bus measurements and analysis functions for dedicated protocols.	
	supported protocols	I²C, SPI, UART, CAN/CAN-FD, LIN, SENT Ethernet(10BASE-T/100BASE-TX), RFFE, Automotive Ethernet (100BASE-T1/1000BASE-T1)
Measurements	field value	allows for the selection of frame types and displays the value of a specified field; the value can be displayed as track and histogram
	frame to frame	measures the distance between the starts of two selectable frame types in seconds
	trigger to frame	measures the distance between the trigger event and the start of a selectable frame type in seconds; alternatively, it measures the distance between the start of a selectable frame type and the trigger event
	frame count	counts the total number of frames in each acquisition
	gap time	measures the distance between the end of a selectable frame type to the start of another selectable frame type in seconds
	bus idle ratio	measures the percentage of idle time on a bus; idle time is defined as the time where the bus is not occupied by frames
	main bit rate	measures the main bit rate of a protocol based on the relevant bits in a frame; if a protocol provides multiple bit rates, the most relevant bit rate is being measured
	secondary bit rate	for protocols with multiple bit rates, the secondary bit rate is available
	frame error count	counts the total number of erroneous frames in each acquisition
	frame error rate	measures the percentage of erroneous frames in relation to the total frames
	consecutive frame error rate	measures the percentage of follow up (consecutive) frame errors, ignoring all single frame errors

R&S®RTO6-K510 low-speed serial busses triggering and decoding

I²C triggering and decoding

Protocol configuration	bit rate	auto-detected
	auto threshold setup	assisted threshold configuration for I²C triggering and decoding
	device list	associate frame address with symbolic ID
Trigger	source (clock and data)	any input channel or logical channel
	bit rate	up to 6.5 Mbps
	trigger event setup	start, stop, restart, missing ACK, address, data, address + data
	address setup	7 bit or 10 bit address (value in hex, decimal, octal or binary); ACK, NACK or either; read, write or either; R/W bit included in address value or apart; condition =, ≠, ≥, ≤, in range, out of range
	data setup	data pattern up to 8 byte (hex, decimal, octal or binary); condition =, ≠, ≥, ≤, in range, out of range; offset within frame in range from 0 byte to 4095 byte

Decode	source (clock and data)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	frame, start/restart, address, R/W bit, data, ACK/NACK, stop, error
	address and data format	hex, decimal, octal, binary, ASCII; symbolic names for user-defined subset of addresses
	decode layer	off, edges, bit
Search	search event setup	combination of start, stop, restart, missing ACK, address, data, address + data
	event settings	same as trigger event settings

SPI triggering and decoding

Protocol configuration	type	2-wire, 3-wire and 4-wire SPI
	bit rate	auto-detected
	bit order	LSB first, MSB first
	word size	4 bit to 32 bit
	frame condition	SS, timeout
	polarity (MOSI, MISO, SS, CLK)	active high, active low
	phase (CLK)	first edge, second edge
	auto threshold setup	assisted threshold configuration for SPI triggering and decoding
Trigger	source (MOSI, MISO, SS, CLK)	any input channel or logical channel
	bit rate	up to 50 Mbps
	trigger event setup	start of frame, MOSI, MISO, MOSI + MISO
	data setup	data pattern up to 256 bit (hex or binary); condition =, ≠; offset within frame in range from 0 bit to 32767 bit
Decode	source (MOSI, MISO, SS, CLK)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	frame, word, error
	data format	hex, decimal, octal, binary, ASCII
	decode layer	edges, bit, words
Search	search event setup	start of frame, MOSI, MISO, MOSI + MISO
	event settings	same as trigger event settings

UART/RS-232/RS-422/RS-485 triggering and decoding

Protocol configuration	bit rate	300 bps to 20 Mbps
	signal polarity	idle low, idle high
	number of bit	5 bit to 9 bit
	bit order	LSB first, MSB first
	parity	odd, even, mark, space, none
	stop bit	1, 1.5 or 2 bit periods
	end of packet	word, timeout, none
	auto threshold setup	assisted threshold configuration for UART triggering and decoding
Trigger	source (TX and RX)	any input channel or logical channel
	trigger event setup	start bit, packet start, data, parity error, break condition
	data setup	data pattern up to 256 bit (hex, decimal, octal, binary or ASCII); condition =, ≠; offset within packet in range 0 bit to 32767 bit
Decode	source (TX and RX)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	packet, data payload, start error, parity error, stop error
	data format	hex, decimal, octal, binary, ASCII

I²S triggering and decoding

Protocol configuration	signal type	I²S standard, left justified, right justified, TDM
	auto threshold setup	assisted threshold configuration for I²S triggering and decoding
Trigger	source	any input channel or logical channel
	trigger event setup	data, window, frame condition, word select, error condition
	data setup	data pattern of an audio channel up to 4 byte (hex, signed decimal, unsigned decimal, octal or binary); condition =, ≠, ≥, ≤, <, >, in range, out of range
	window setup	word count of data pattern of an audio channel up to 4 byte (hex, signed decimal, unsigned decimal, octal or binary); condition =, ≠, ≥, ≤, <, >, in range, out of range
	frame condition setup	combination of audio channels in a frame, up to 4 byte (hex, signed decimal, unsigned decimal, octal or binary); condition =, ≠, ≥, ≤, <, >, in range, out of range
	word select setup	rising or falling edge of word select input channel
	error condition setup	source of word select
Decode	source	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus and logical signal, tabulated list
	color coding	audio frame, frame error, incomplete frame
	data format	hex, unsigned decimal, signed decimal (two's complement), octal, binary, ASCII
Protocol measurements	audio display	display of audio waveform for specified audio channels
	long-term display	history of selected audio data as trace against measurements, waveforms and time index

Manchester and NRZ triggering and decoding

Protocol configuration	signal type	selectable, one channel, differential or single-ended, two channel, differential or single-ended
	bit rate	auto detected, adjustable
	auto threshold setup	assisted threshold configuration
	source	analog, math. channels, logical (only NRZ)
	bit encoding variants	Manchester, Manchester II, NRZ clocked, NRZ unclocked
	properties	active state (high/low), idle state (high/low), clock edge (first/second)
	frame separation	gap, enable signal (only NRZ)
Frame format	frame	multiple frame management, frame identification and sync, variable length frames, variable number of cells
	cells	name, size (bit), numeric format, bit order, color
	file storage of frame format	save/load as xml files

Trigger	variants	all supported bit encodings
	trigger event setup	frame start
		pattern
		advanced trigger
	frame start	gap, start bit
	pattern	up to 256 bit pattern within 65 535 bit frame [13]
	advanced trigger	frame type (with OR combinations), frame fields (with AND combinations), frame field data; conditions =, ≠, <, ≤, >, ≥, in range, out of range for data count, word count, data value; error types
Decode	display type	decoded bus, logical signal, bus signal, tabulated list, result details, decode layers
	color coding	according to cell configuration table
	data format	according to cell configuration table
	decode layer	edges, binary
Search	event settings	same as advanced trigger settings
Filter	The filter function selects those decode events that shall be shown in the result table. Events that do not match the criteria set will not be displayed in the table when the filter is turned on.	
	settings	same as advanced trigger settings

R&S®RTO6-K520 automotive protocols triggering and decoding

CAN/CAN FD triggering and decoding

Protocol configuration	signal type	CAN_H, CAN_L
	standard (CAN FD)	ISO, non-ISO (Bosch)
	bit rate (CAN)	100 bps to 1 Mbps
	bit rate (CAN FD)	
	arbitration rate	10 kbps to 1 Mbps
	data rate	10 kbps to 15 Mbps
	sampling point	5 % to 95 % within bit period; independent settings for arbitration phase and data phase
	device list	associate frame identifier with symbolic ID, load DBC file content
	auto threshold setup	assisted threshold configuration
Trigger	source	any input channel or logical channel
	trigger event setup	start of frame, frame type, identifier, identifier + data, symbolic, error condition (any combination of CRC error, bit stuffing error, form error and ACK error)
	identifier setup	frame type (data, remote or both), identifier type (standard or extended); condition =, ≠, ≥, ≤, in range, out of range
	FD bit	FDF, BRS and ESI (0, 1, X)
	data setup	data pattern up to 8 byte in the complete data range (hex, decimal, octal or binary); big-endian or little-endian; condition =, ≠, ≥, ≤, in range, out of range
	symbolic setup	message name, signal name; numeric signal condition =, ≠, ≥, ≤, in range, out of range; enumerated signal condition =, ≠, ≥, ≤

[13] The pattern trigger will not be effective after Manchester violations.

Decode	source	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	start of frame, identifier, FD bit, DLC, data payload, CRC, end of frame, error frame, overload frame, CRC error, bit stuffing error
	data format	hex, decimal, octal, binary, ASCII, symbolic
Search	source	any input channel or logical channel
	search event setup	combination of start of frame, frame type, identifier, identifier + data, error condition (any combination of CRC error, bit stuffing error, form error and ACK error) or only symbolic
	event settings	same as trigger event settings

CAN XL triggering and decoding

Protocol configuration	signal type	CAN_H, CAN_L
	bit rate	
	nominal bit rate	100 kbps to 1 Mbps
	FD data rate	100 kbps to 15 Mbps
	XL data rate	100 kbps to 30 Mbps
	sampling point	30 % to 90 % within bit period; independent settings for nominal bit rate, FD data rate and XL data rate
	device list	associate frame identifier with symbolic ID, load DBC file content
Trigger (software based)	primary event trigger (hardware based)	edge
	frame type	CBFF, CBFF-R, CEFF, CEFF-R, FBFF, FEFF, XLFF, overload, error
	CBFF	ID, DLC; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data index: selects the specific dataword; conditions =, in range
	CBFF-R	ID, DLC; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options
	CEFF	EXT-ID, DLC; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data index: selects the specific dataword; conditions =, in range
	CEFF-R	EXT-ID, DLC; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options
	FBFF	ID, DLC; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; BRS, ESI; value 0, 1 for each of these options; data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data index: selects the specific dataword; conditions =, in range

	FEFF	ID, DLC; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; BRS, ESI; value 0, 1 for each of these options; data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data index: selects the specific dataword; conditions =, in range
	XLFF	Priority ID, SDT, DLC, VCID, AF; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; SEC; value 0, 1; data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data index: selects the specific dataword; conditions =, in range
	error condition	EOF, ack delimiter, no ack, CRC delimiter, CRC, stuff count, form, bit stuffing, unknown
Decode	source	any analog or logical input channel; math or reference waveform
	display type	decoded bus, tabulated list
	color coding	start of frame, identifier, DLC, ADS, SDT, VCID, AF, data payload, CRC, end of frame, error frame, overload frame, CRC error, bit stuffing error
	data format	hex, decimal, octal, binary, ASCII, symbolic
	result export	export of all result data into CSV, XML, HTML and Py file formats
Search	settings	same as trigger settings

LIN triggering and decoding

Protocol configuration	version	1.3, 2.x or SAE J602; mixed traffic is supported
	bit rate	standard bit rate (1.2/2.4/4.8/9.6/10.417/19.2 kbps) or user-defined bit rate in range from 1 kbps to 20 kbps
	device list	associate frame identifier with symbolic ID, data length and protocol version
	auto threshold setup	assisted threshold configuration for LIN triggering and decoding
Trigger	source	any input channel
	trigger event setup	start of frame (sync break), identifier, identifier + data, wake-up frame, error condition (any combination of checksum error, parity error and sync field error)
	identifier setup	range from 0d to 63d; select condition =, ≠, ≥, ≤, in range, out of range for trigger “identifier”; select single identifier and condition = for trigger “identifier + data”
	data setup	data pattern up to 8 byte (hex, decimal, octal or binary); condition =, ≠, ≥, ≤, in range, out of range
Decode	source (TX and RX)	any input channel, math waveform, reference waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	frame, frame identifier, data payload, checksum, error condition
	data format	hex, decimal, octal, binary, ASCII

Search	search event setup	combination of start of frame (sync break), identifier, identifier + data, wake-up frame, error condition (any combination of checksum error, parity error and sync field error)
	event settings	same as trigger event settings

FlexRay triggering and decoding

Protocol configuration	signal type	single-ended, differential, logic
	channel type	channel A, channel B
	bit rate	standard bit rates (2.5/5.0/10.0 Mbps)
	device list	associate frame identifier with symbolic ID
	auto threshold setup	assisted threshold configuration for FlexRay triggering and decoding
	source	any input channel or logical channel
Trigger	trigger event setup	start of frame, header + data, symbol, wake-up, error condition (any combination of FSS error, BSS error, FES error, header CRC error and frame CRC error)
	header setup	indicator bits, identifier, payload length, cycle count
	indicator bits setup	payload preamble bit, null frame bit, sync frame bit and startup frame bit separately configurable (1, 0 or don't care)
	identifier setup	condition =, ≠, ≥, ≤, in range, out of range
	payload length setup	condition =, ≠, ≥, ≤, in range, out of range
	cycle count	condition =, ≠, ≥, ≤, in range, out of range; step parameter for selection of non-contiguous values within provided range
	data setup	data pattern up to 8 byte (hex, decimal, octal or binary); condition =, ≠, ≥, ≤, in range, out of range; offset within frame in range from 0 byte to 253 byte
Decode	source	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	frame, frame header, identifier, payload length, header CRC, cycle count, data payload, frame CRC, error condition
	data format	hex, decimal, octal, binary, ASCII
Search	search event setup	combination of start of frame, header + data, symbol, wake-up, error condition (any combination of FSS error, BSS error, FES error, header CRC error and frame CRC error)
	event settings	same as trigger event settings

SENT triggering and decoding

Protocol configuration	signal type	data signal
	clock period (clock tick)	1 µs to 100 µs
	clock tolerance	0 % to 25 %
	data nibbles	1 to 6
	serial message type	none, short serial message and enhanced serial message
	CRC version	Legacy (Feb 2008) and v2010 (Latest)
	CRC calculation	SAE J2716 standard and TLE 4998X
	pause pulse	no, yes, for constant frame length
	frame length in clock ticks (applicable only when pause pulse = constant frame length)	104 to 922

Trigger	source	any analog input channel
	trigger event setup	calibration or sync, transmission sequence, serial message and error condition
	transmission sequence status nibble setup	from 0 to F, condition =, ≠, ≥, ≤, in range, out of range
	transmission sequence data nibbles setup	each nibble value from 0 to F, condition =, ≠, ≥, ≤, in range, out of range
	serial message identifier setup	from 00 to FF, condition =, ≠, ≥, ≤, in range, out of range
	serial message identifier type setup (applicable only when the serial protocol = enhanced serial message in protocol configuration)	4 bit and 8 bit
	serial message data setup	00 to FF (short serial message) 000 to FFF (enhanced serial message with 8 bit ID) 0000 to FFFF (enhanced serial message with 4 bit ID)
	error condition setup	form error, calibration pulse error, pulse period error, CRC error and irregular frame length error
Decode	source	any analog input channel,
	display type	decoded bus, tabulated list
	color coding	transmission sequence: sync/calibration, status, data bits, CRC, pause pulse (optional), calibration pulse error, pulse period error, irregular frame length error and CRC error; serial message: identifier, data, CRC, form error, CRC error
	data format	hex, decimal, octal, binary, ASCII
Search	source	any analog input channel
	search event setup	calibration or sync, transmission sequence, serial message and error condition
	event settings	same as trigger event settings

CXPI triggering and decoding

Protocol configuration	signal type	one channel
	bit rate	auto-detected/adjustable
	auto threshold setup	assisted threshold configuration
	source (SDATA)	any input channels, math waveforms, reference waveforms or logical channels
Trigger	trigger event setup	frame start
		frame types with frame content
		error condition
	frame types	normal, normal poll, sleep, long, long poll, PID, PTYPE, PTYPE+PID
	frame content (depending on frame type)	frame ID, NW, CT, DLC, data pattern
	data pattern setup	up to 8 byte (condition =, ≠, <, >, ≥, ≤, in range, out of range), payload data index (=, <, >, ≥, ≤, range)
	error condition setup	IFS, IBS, CRC, length, parity, UART, DLC
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, details, decode layers
	color coding	for different cell types
	data format	hex, octal, binary, signed, unsigned
Search	search event setup	frame start
		frame types with data
		error types
	event settings	same as trigger event settings

R&S®RTO6-K530 aerospace protocols triggering and decoding

MIL-STD-1553 triggering and decoding

Protocol configuration	signal type	single-ended
	bit rate	standard bit rate (1 Mbit/s)
	polarity	normal, inverted
	device list	associate frame identifier with symbolic ID
	auto threshold setup	assisted threshold configuration
	timing	min. gap (2 µs to 262 µs) or off; max. response (2 µs to 262 µs) or off
Trigger	trigger event setup	sync, word, data word, command/status word, command word, status word, error condition
	sync and word setup	all words, command/status word, data word
	data word setup	RTA (condition =, ≠, ≥, ≤, in range, out of range); data pattern (condition =, ≠, ≥, ≤, in range, out of range); payload data index (=, <, >, ≥, ≤, range); max length of data pattern is 4 byte
	command/status word setup	RTA (condition =, ≠, ≥, ≤, in range, out of range); 11 bit pattern (condition =, ≠, ≥, ≤, in range, out of range)
	command word setup	RTA (condition =, ≠, ≥, ≤, in range, out of range); subaddress/mode (condition =, ≠, ≥, ≤, in range, out of range); data word count/mode count (condition =, ≠, ≥, ≤, in range, out of range); direction (T/R)
	status word	RTA (condition =, ≠, ≥, ≤, in range, out of range); status flags (message error, instrumentation, service request, broadcast command, busy, subsystem flag, dynamic bus control, terminal flag)
	error condition	any combination of sync error, Manchester error, parity error, timing error (see protocol configuration)
Decode	source	any analog input channel, math waveform, reference waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	frame (word), sync, RTA, status bit field, parity, data field, error condition
	data format	hex, octal, binary, ASCII, signed, unsigned
Search	search event setup	sync, word, data word, command/status word, command word, status word, error condition
	event settings	same as trigger event settings

ARINC 429 triggering and decoding

Protocol configuration	signal type	single-ended
	bit rate	high (100 kbit/s)
		low (12 kbit/s to 14.5 kbit/s)
	polarity	A leg, B leg
	device list	associate frame identifier with symbolic ID
	auto threshold setup	assisted threshold configuration
	timing	min. gap (0 bit to 100 bit) or off; max. gap (0 bit to 1000 bit) or off
Trigger	trigger event setup	word start, word stop, label + data, error condition
	label + data setup	label (condition =, ≠, ≥, ≤, in range, out of range); data (condition =, ≠, ≥, ≤, in range, out of range); SDI/SSM
	error condition	any combination of coding error, parity error, timing error (see protocol configuration)

Decode	source	any analog input channel, math waveform, reference waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	frame (word), label, SDI, data, SSM, parity, error condition
	data format	hex, octal, binary, ASCII, signed, unsigned
Search	search event setup	word start, word stop, label + data, error condition
	event settings	same as trigger event settings

SpaceWire triggering and decoding

Protocol configuration	signal type	two channels: strobe and data (differential or single-ended)
	bit rate	auto adjust (strobe + data)
	source	any analog input channels, logical channels [14], math channels, reference channels
Trigger	trigger event setup	control frame, data pattern, null frame, time code, error condition
	control frame setup	any, FCT, EOP, EEP
	data pattern setup	8 bit (condition =, ≠, <, >, ≥, ≤, in range, out of range)
	time code setup	8 bit (condition =, ≠, <, >, ≥, ≤, in range, out of range)
	errors condition setup	parity, ESC
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	control frame, data frame, null frame, time code
	data format	hex, octal, binary, signed, unsigned
Search	search event setup	control frame, data pattern, null frame, time code, error
	event settings	same as trigger event settings

R&S®RTO6-K540 Ethernet protocols triggering and decoding

Ethernet (10BASE-T/100BASE-TX) triggering and decoding

Protocol configuration	signal type	one differential channel
	bit rate	auto-detected
	auto threshold setup	assisted threshold configuration
	full autoset	adjust horizontal and vertical resolution and perform auto threshold
	source (SDATA)	analog and math channels
	variants	10BASE-T, 100BASE-TX
Trigger	frame start	trigger at start of any MAC frame
	pattern	fast trigger for 10BASE-T MAC frames, 32 byte, index 0 to 65535
	frame	advanced trigger configuration for MAC frames only 48 bit destination address, 48 bit source address, 16 bit length/type, 32 bit frame check; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	error	preamble error, length error, CRC error

[14] SpaceWire protocol trigger on logical channels is not available.

Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, details, decode layers
	color coding	preamble, frame, destination address, source address, data
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, binary
	result export	export of all result data into CSV, XML, HTM and PY file formats
Search	search event setup	frame, error
	event settings	same as trigger event settings

MDIO triggering and decoding

Protocol configuration	bit rate	up to 5 Mbps (auto-detected)
	auto threshold setup	assisted threshold configuration for MDIO triggering and decoding
	device list	associate frame address with symbolic ID
Trigger	source (clock and data)	any input channel or logical channel
	trigger event setup	start, stop, ST, OP, PHY address, register address, data
	ST setup	01 (clause 22), 00 clause 45, any
	OP setup	address, write, post read, read, any
	PHY address setup	5 bit address (hex, decimal, octal or binary); equal
	PHY register (clause 22)/device type (clause 45) setup	5 bit value (hex, decimal, octal or binary); equal
	data (clause 22)/data/address (clause 45)	16 bit value (hex, decimal, octal or binary); equal
Decode	source (clock and data)	any input channel, math waveform, reference waveform, logical channel
	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	frame, PHY address, PHY register, address, data, turnaround
	PHYAD/PRTAD	symbolic names for user-defined addresses
	address/data field format	hex, decimal, octal, binary, ASCII
	decode layer	edges, binary
Search	source (clock and data)	any input channel, math waveform, reference waveform, logical channel
	search event setup	start, stop, ST, OP, PHY address, register address, data
	event settings	same as trigger event settings

R&S®RTO6-K550 MIPI low speed triggering and decoding

RFFE triggering and decoding

Protocol configuration	signal type	two channel, single-ended
	bit rate	auto-detected
	auto threshold setup	assisted threshold configuration
	full autoset	full autoset of horizontal and vertical settings and auto threshold setup
	source (SCLK, SDATA)	any two input channels, math waveforms, reference waveforms, or logical channels
	supported version	1.X, 2.0,2.1 and 3.0
	read mode	standard or read mode
	glitch filter	configurable glitch filter
	gap detection	detect gaps between sequences

Trigger	trigger event setup	sequence start, sequence stop, register 0 write, register write, register read, extended register write, extended register read, extended register write long, extended register read long, error condition types
	sequence start setup	4 bit slave address; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	sequence stop setup	4 bit slave address; conditions =, ≠, <, ≤, >, ≥, in range, out of range
	register 0 write setup	4 bit slave address, 7 bit data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options
	register write/read	4 bit slave address, 5 bit register address, 8 bit data word; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options
	extended register write/read	4 bit slave address; 8 bit address, byte count: 0 to 15 (inclusive), data pattern: 1 to 16 byte (hex or binary); conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; index: 1 to 16 selects the specific data frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	extended register write long/read long	4 bit slave address, 8 bit address, byte count: 0 to 7 (inclusive), data pattern: 0 to 8 byte (hex or binary); conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; index: 1 to 8 selects the specific data frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	interrupt summary and notification	4 bit slave address, bit count 0 to 32, notification and interrupt bits
	masked write	4 bit slave address; 8 bit address, 8 bit mask, 8 bit data pattern; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	master ownership handover	2 bit MID; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	master write/read	2 bit MID, 8 bit address, 16 bit data pattern; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	master context transfer write/read	2 bit MID, 8 bit byte count, 8 bit address, data pattern: 1 to 8 byte (hex or binary); conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; index: 1 to 256 selects the specific data frame byte; conditions =, ≠, <, ≤, >, ≥, in range
	error condition	SSC error; length error, bus park error, parity error, no response, unknown sequence, version error, min. gap between frames: 1 ns to 10 us

Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, decode layers
	color coding	sequence, frame, error
	data format	hex, octal, binary, ASCII, signed, unsigned
	decode layer	off, edges, bit
Search	search event setup	sequence start, sequence stop, register 0 write, register write, register read, extended register write, extended register read, extended register write long, extended register read long, master read, master write, master ownership handover, interrupt summary and notification, error condition types
	event settings	same as trigger event settings

I³C triggering and decoding

Protocol configuration	signal type	two channel, single-ended
	bit rate	auto detected
	source (SCL, SDA)	any analog or logical input channel; math or reference waveform
	gap detection	support frame detection with gap definition
Trigger (software based)	primary event trigger (hardware based)	edge
	frame type	I³C probe, read, write, CCC broadcast, CCC direct, HDR-DDR, HDR-ternary
	I³C probe	reserved; conditions =, ≠, <, ≤, >, ≥, in range, out of range; R/W; value 0, 1 ACK; value 0, 1
	read	address; conditions =, ≠, <, ≤, >, ≥, in range, out of range; R/W; value 0, 1 ACK-A; value 0, 1 data; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data index: selects the specific dataword; conditions =, in range
	write	address; conditions =, ≠, <, ≤, >, ≥, in range, out of range; R/W; value 0, 1 ACK-A; value 0, 1 data; conditions =, ≠, <, ≤, >, ≥, in range, out of range for each of these options; data index: selects the specific dataword; conditions =, in range
	CCC broadcast	reserved; conditions =, ≠, <, ≤, >, ≥, in range, out of range; R/W; value 0, 1 ACK-A; value 0, 1 ccc; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data index: selects the specific dataword; conditions =, in range
	CCC broadcast	reserved; conditions =, ≠, <, ≤, >, ≥, in range, out of range; R/W; value 0, 1 ACK-A; value 0, 1 ccc; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data index: selects the specific dataword; conditions =, in range

	HDR-DDR	command; conditions =, ≠, <, ≤, >, ≥, in range, out of range; address; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data index: selects the specific dataword; conditions =, in range p; conditions =, ≠, <, ≤, >, ≥, in range, out of range; p index: selects the specific data word; conditions =, in range crc; conditions =, ≠, <, ≤, >, ≥, in range, out of range;
	HDR-ternary	R/W; value 0, 1 command; conditions =, ≠, <, ≤, >, ≥, in range, out of range; address; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data; conditions =, ≠, <, ≤, >, ≥, in range, out of range; data index: selects the specific dataword; conditions =, in range p; conditions =, ≠, <, ≤, >, ≥, in range, out of range; p index: selects the specific data word; conditions =, in range
	error condition	ACK, parity, CRC, length, unknown
Decode	source (clock and data)	any input channel, logical channel
	display type	decoded bus, tabulated list
	color coding	frame, field types, status
	data format	hex, decimal, octal, binary, ASCII
	result export	export of all result data into CSV, XML, HTML and Py file formats
Search	settings	same as trigger settings, where applicable

R&S®RTO6-K560 automotive Ethernet triggering and decoding

Ethernet (10BASE-T1S) triggering and decoding

Protocol configuration	source	any analog input channel, math or reference waveform
	threshold	upper/lower
Trigger (software based)	primary event trigger (hardware based)	edge
	frame type	MAC, COMMIT, BEACON or unknown
	MAC frame setup	destination address (condition =, ≠, <, >, ≥, ≤, in range, out of range), source address (condition =, ≠, <, >, ≥, ≤, in range, out of range), length/type (condition =, ≠, <, >, ≥, ≤, in range, out of range), data (condition =, ≠, <, >, ≥, ≤, in range, out of range), data index (condition =, in range)
	error condition setup	preamble, SFD, ESD, CRC
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	for different cell types
	data format	hex, decimal, octal, binary, signed, unsigned, ASCII
	decode layer	reversed bits, descrambled bits, ternary symbols
	result export	export of all result data into CSV, XML, HTML and Py file formats
Search	settings	same as trigger settings, where applicable

Ethernet (100BASE-T1) triggering and decoding

Protocol configuration	signal type	one channel differential, two channels single-ended, optional additional use of reverse channels for signal improvement: one channel differential, two channels single-ended
	symbol rate	66.667 Msymbol/s, adjustable for testing
	thresholds	upper/lower, assisted threshold configuration
	source	any analog input channels, math waveforms, reference waveforms
	polarity	normal, inverted
	mode	slave, master
Trigger	trigger event setup	frame start
		MAC frame
		idle frame
		error conditions
	MAC frame setup	destination address (condition =, ≠, <, >, ≥, ≤, in range, out of range), source address (condition =, ≠, <, >, ≥, ≤, in range, out of range), length/type (condition =, ≠, <, >, ≥, ≤, in range, out of range), frame check (condition =, ≠, <, >, ≥, ≤, in range, out of range), data (condition =, ≠, <, >, ≥, ≤, in range, out of range), data index (condition =, <, >, ≥, ≤, range)
	error condition setup	preamble error, CRC error, SFD error
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	for different cell types
	data format	hex, octal, binary, signed, unsigned
	decode layer	reversed bit, descrambled bit, scrambled bit, ternary symbols
	result export	export of all result data into CSV, XML, HTM and PY file formats
Search	search event setup	frame start
		MAC frame
		idle frame
		error conditions
	event settings	same as trigger event settings

Ethernet (1000BASE-T1) triggering and decoding

Protocol configuration	signal type	one channel differential, two channels single-ended, optional additional use of reverse channels for signal improvement: one channel differential, two channels single-ended
	symbol rate	750 Msymbol/s, adjustable for testing
	thresholds	automatically adjusted during decoding
	source	any analog input channels, math waveforms, reference waveforms
	polarity	normal, inverted
	mode	slave, master
Trigger	trigger event setup	frame start
		MAC frame
		idle frame
		error conditions
	MAC frame setup	destination address (condition =, ≠, <, >, ≥, ≤, in range, out of range), source address (condition =, ≠, <, >, ≥, ≤, in range, out of range), length/type (condition =, ≠, <, >, ≥, ≤, in range, out of range), frame check (condition =, ≠, <, >, ≥, ≤, in range, out of range), data (condition =, ≠, <, >, ≥, ≤, in range, out of range), data index (condition =, <, >, ≥, ≤, range)
	error condition setup	RS-FEC error, out of range error, CRC error, SFD error
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	for different cells types
	data format	hex, octal, binary, signed, unsigned
	decode layer	ternary symbols, scrambled bit, descrambled bit, corrected RS-FEC symbols
	result export	export of all result data into CSV, XML, HTM and PY file formats
Search	search event setup	frame start
		MAC frame
		idle frame
		error conditions
	event settings	same as trigger event settings

R&S®RTO6-K570 USB protocols triggering and decoding

USB 1.0/1.1/2.0 triggering and decoding

Protocol configuration	signal type	single-ended, differential
	protocol type	low, full, high speed and HSIC
	bit rate	standard bit rates (1.5/12/480 Mbit/s)
	source	any input channel
	probe type	
	for low and full speed	single-ended probe
	for high speed	differential probe (R&S®RT-ZDx)
	for HSIC	single-ended probe(R&S®RT-ZSx)
	auto threshold setup	assisted threshold configuration for USB triggering and decoding

Trigger	trigger event setup	start of packet, end of packet, PID token (IN, OUT, SETUP, SOF), PID data (Data0, Data1, Data2 [15], MData [15]), PID handshake (ACK, NAK, STALL, NYET [15]), PID special (PRE [16], ERR [15], SPLIT [15], PING [15]); bus state (reset [16], resume [16], suspend [16]); error condition
	address, endpoint and frame setup SC, port, SEU, ET check (SPLIT) [16]	condition =, ≠, ≥, ≤, in range, out of range
	data setup	data pattern up to 4 byte (hex, decimal, octal, binary or ASCII), bit separately configurable (1, 0 or don't care); condition =, ≠; position based or window based triggering (first occurrence in packet payload)
	error condition	any error, PID error, CRC5 error, CRC16 error, bit stuffing error, unexpected PID, SE1 error [16] and glitching error
Decode	source	any input channel, math waveform
	display type	decoded bus, logical signal, bus + logical signal, tabulated list
	color coding	packet identifier, payload length, frame, address, endpoint, data payload, CRC5, CRC16, error condition
	data format	hexadecimal, decimal, octal, binary, ASCII, unsigned
Search	search event setup	combination of start of packet, PID token (IN, OUT, SETUP, SOF), PID data (Data0, Data1, Data2 [15], MData [15]), PID handshake (ACK, NAK, STALL, NYET [15]), PID special (PRE [16], ERR [15], SPLIT [15], PING [15]); error condition (any error, PID error, CRC5 error, CRC16 error, bit stuffing error, unexpected PID, SE1 error [16] and glitching error)
	address, endpoint and frame setup SC, port, SEU, ET check (SPLIT)	condition =, ≠, ≥, ≤, in range, out of range
	data setup	data pattern up to 4 byte (hex, decimal, octal, binary or ASCII), bit separately configurable (1, 0 or don't care); condition =, ≠; position based or window based triggering (first occurrence in packet payload)
	error condition	any error, PID error, CRC5 error, CRC16 error, bit stuffing error, unexpected PID, SE1 error [16] and glitching error

USB 3.1 Gen 1 triggering and decoding

Suitable for 6 GHz models only.

Protocol configuration	signal type	one channel
	bit rate	auto detected
	auto threshold setup	supported
	source	any analog input channels, math channels, reference channels
	scrambling	selectable
	digital signal processing	CTLE continuous time equalizer, DFE decision feedback equalizer

[15] Only available in high speed and HSIC.
[16] Only available in low and full speed.

Trigger	trigger event setup	frame start
		frame content
		errors
	frame content	USB packet types: TSEQ, TSET1, TSET2, set link function, U2 inactivity timeout, vendor device test, port capability, port configuration, port, config. resp., link delay meas, ACK, NRDY, ERDY, STATUS, STALL, function wake, latency tolerance, bus interval, adjust, host role request, sublink speed, ping, ping response, data packet header, data packet payload, DPP aborted, isochronous timestamp, link command, info, BRST, BDAT, BERC, BCNT, idle; fields according to selected USB packet with content conditions =, ≠, <, >, ≥, ≤, in range, out of range
	errors	CRC, length, value out of range
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	cell and frame types
	data format	hexadecimal, octal, binary, ASCII, signed, unsigned, 8b/10b symbols
	decode layer	edges, bit, scrambled symbols, descrambled symbols, byte
	result export	export of all result data into CSV, XML, HTM and PY file formats
Search	search event setup	frame start
		frame content
		errors
	event settings	same as trigger event settings

USB power delivery triggering and decoding

Protocol configuration	signal type	one channel
	bit rate	auto detected
	source	any analog input channel, logical channels, math channels, reference channels
	thresholds	data, advertisements
	data details	detailed breakdown selectable
Trigger	trigger event setup	frame start
		frame content
		errors
	frame content	extended, NumDataObjs, MsgID, PwrRole/Plug, Rev, DataRole, MsgType, voltage advertisements (content conditions =, ≠, <, >, ≥, ≤, in range, out of range)
	errors	4b/5b, preamble, CRC, length, SOP warning
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, details, decode layers
	color coding	cell and frame types
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, 4b5b symbols
Search	search event setup	frame start
		frame content
		errors
	event settings	same as trigger event settings

USB 3.1 SSIC triggering and decoding

Protocol configuration	signal type	up to 4 lanes differential
	bit rate	auto detected
	source	any analog input channels, math channels, reference channels
	scrambling	selectable
	digital signal processing	CTLE continuous time equalizer, DFE decision feedback equalizer
Trigger	trigger event setup	frame start
		frame content
		errors
	frame content	USB packet types: TSEQ, TSET1, TSET2, set link function, U2 inactivity timeout, vendor device test, port capability, port configuration, port, config. resp., link delay meas, ACK, NRDY, ERDY, STATUS, STALL, function wake, latency tolerance, bus interval, adjust, host role request, sublink speed, ping, ping response, data packet header, data packet payload, DPP aborted, isochronous timestamp, link command, info, BRST, BDAT, BERC, BCNT, idle; fields according to selected USB packet with content conditions =, ≠, <, >, ≥, ≤, in range, out of range
	errors	CRC, length, value out of range
Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	cell and frame types
	data format	hex, octal, binary, signed, unsigned
	decode layer	edges, bit, byte, 8b/10b symbols, LCC bit, descrambler, lane merge
Search	search event setup	frame start
		frame content
		errors
	event settings	same as trigger event settings

R&S®RTO6-K580 MIPI high speed triggering and decoding

MIPI D-PHY triggering and decoding

Protocol configuration	signal type	clock, data (differential or single-ended)
	bit rate	selectable without clock lane (1 Mbps to 2.5 Gbps), auto detect with clock lane
	source	any input channels, math waveforms, reference waveforms
	variants	D-PHY v. 1.2, CSI-2 v.1.2, DSI v. 1.3
Trigger	trigger event setup	HS start of packet, HS end of packet, HS packet header, HS data, LP escape mode, LP lane turnaround, LP HS request
	HS packet header setup	virtual channel, data type, word count; conditions =, ≠, <, ≤, >, ≥, in range, out of range for data and word count
	HS data	virtual channel, data type, word count, data value, data index; conditions =, ≠, <, ≤, >, ≥, in range, out of range for data count, word count, data value
	LP escape mode	escape mode, data value, data index; conditions =, ≠, <, ≤, >, ≥, in range, out of range for escape mode and data value

Decode	display type	decoded bus, tabulated list, details, decode layers
	color coding	high speed: frames according to trace, cells; low power: escape word, data word
	data format	hex, octal, binary, signed, unsigned
	decode layer	off, HS edges, HS binary, HS burst bit, HS burst byte, HS merged byte, HS merged words, LP edges, LP states, LP active states, LP binary
	result export	export of all result data into CSV, XML, HTM and PY file formats
Search	search event setup	HS start of packet, HS end of packet, HS packet header, HS data, LP escape mode, LP lane turnaround, LP HS request
	event settings	same as trigger event setup

MIPI M-PHY triggering and decoding

Protocol configuration	signal type	up to 4 channels, differential
	bit rate	clock recovery
	source (SDATA)	analog and math channels, reference waveforms
	variants	UniPro 1.6 and M-PHY 4.0
Trigger	trigger event setup	M-PHY burst, M-PHY adapt, M-PHY LCC, UniPro DL_PDU frames, UniPro PACP frames, UniPro trigger upper frames, M-PHY/UniPro errors
Decode	display type	decoded bus, logical signal, bus + logical signal, tabulated list, details, decode layers
	color coding	for different cells/frame types
	data format	K/D symbols; with UniPro additionally: hex, octal, binary, signed, unsigned
	decode layer	off, edges, bit, 8b/10b synbols, LCC bit; with UniPro additionally: filter/descrambler, lane merge, byte
Search	search event setup	M-PHY burst, M-PHY adapt, M-PHY LCC, UniPro DL_PDU frames, UniPro PACP frames, UniPro trigger upper frames, M-PHY/UniPro errors

R&S®RTO6-K590 PCI express triggering and decoding

8b10b triggering and decoding

Protocol configuration	signal type	one/two channel, differential, single-ended
	bit rate	selectable/adjustable auto configuration
	auto threshold setup	assisted threshold configuration
	one click setup	convenient way for perfect decode results; auto scaling of waveforms, auto threshold and bitrate estimation on one click
	source (differential, single-ended D+/D–)	full combination of either analog, math, reference channels
	variants	all layer 1 (physical layer) encoded 8b/10b protocols, recommended for Ethernet, FibreChannel 1G, 2G, PCI Express®, Serial ATA, Serial Rapid IO (SRIO), XAUI
Trigger	trigger event setup	symbols, errors
	symbols	K/D symbol (8 bit/10 bit), complex expression (combination of K/D symbols, wildcards, disparity)
	errors	disparity, glitching and unknown symbol
Decode	display type	decoded bus, bus signal, tabulated list, details, decode layers
	color coding	sync symbol, K symbols, data (Dx.y) coding and error coding
	data format	hex, 10 bit and K/D representation
	decode layer	edges, bit
Search	search event setup	symbols, errors
	event settings	same as trigger event settings

PCI Express 1.1/2.0 triggering and decoding

Suitable for 6 GHz models only.

Protocol configuration	signal type	up to four channels (×1, ×2, ×4 link size) differential signals
	bit rate	predefined 2.5 Gbit/s for Gen 1 and 5 Gbit/s for Gen 2
	source	any analog input channels, math channels, reference channels
	clock data recovery	PLL based CDR, PLL order, damping factor, bandwidth, rel. bandwidth
	digital signal processing	CTLE continuous time equalizer, DFE decision feedback equalizer

Trigger	trigger event setup	TLP (transaction layer packets), DLLP (data layer packets), ordered sets, errors
	TLP (transaction layer packets)	any type, memory request (32 bit/64 bit, R/W, ordering, snoop, seq. number, Requester ID), I/O transactions, configuration requests, message requests (incl. routing and message code), completion packets (status, completer ID), atomic operation (FetchAdd, SWAP, CAS) for 32 bit/64 bit
	DLLP (data layer packets)	any type, Ack and Nak (seq. number), InitFC1, InitFC2, updateFC (credit type C, NP, Cpl and virtual channel), power management with PM type, vendor packet format. multi-root I/O virtualization (MRDLLP): MRInit (phase, VH FC, mixed type, authorized, device/port type), MRReset (A, VH Group), MRUpdateFC, MRInitFC1 and MRInitFC2 (VL number, VH absent, TLP type, credit type)
	ordered sets	SKP OS, training sequence (TS1, TS2), fast training sequence (FTS), electrical idle OS, electrical idle exit OS, compliance and modified compliance pattern
	errors condition setup	CRC16, ECRC, LCRC, disparity, invalid packets (corrupt header or length errors)
Decode	display type	decoded bus, tabulated list, decode layers, detailed result display for packets
	color coding	TLP, DLLP, K-code, D-code, ordered sets, errors
	data format	K/D symbol, 8 bit format (hex)
	decode layer	8b10b, descrambled 8b10b, bit
	result export	export of all result data into CSV, XML, HTM and PY file formats
Search	search event setup	TLP, DLLP, ordered sets, errors
	event settings	same as trigger event settings

Ordering information

Designation	Type	Order No.
Base unit (including standard accessories: 500 MHz passive probe (10:1) per channel, accessories bag, quick start guide, CD with manual, power cord)		
Oscilloscope		
Base unit, 200 Mpoints/800 Mpoints, 4 channels, bandwidth option required	R&S®RTO64	1802.0001.04
Bandwidth options		
600 MHz, 10 Gsample/s	R&S®RTO6-B90	1802.0182.02
1 GHz, 10 Gsample/s	R&S®RTO6-B91	1802.0199.02
2 GHz, 10 Gsample/s	R&S®RTO6-B92	1802.0201.02
3 GHz, 10 Gsample/s	R&S®RTO6-B93	1802.0218.02
4 GHz, 20 Gsample/s	R&S®RTO6-B94	1802.0224.02
6 GHz, 20 Gsample/s	R&S®RTO6-B96	1802.0230.02
Hardware options (plug-in)		
Mixed signal option, 400 MHz, 5 Gsample/s, 16 channels	R&S®RTO6-B1	1801.6741.02
Digital extension port for R&S®RT-ZVC usage with R&S®RTO6 oscilloscope, included in R&S®RTO6-B1	R&S®RTO6-B1E	1801.6735.02
Arbitrary waveform generator, 100 MHz, 2 analog channels, 8 bit pattern generator	R&S®RTO6-B6	1801.6758.02
16 GHz differential pulse source	R&S®RTO6-B7	1801.6764.02
GPIB interface	R&S®RTO6-B10	1801.6770.02
Replacement solid state disk		
For R&S®RTO6 with Windows 10 operation system	R&S®RTO6-B19	1801.6787.02
For R&S®RTO6 with Windows 11 operation system	R&S®RTO6-B19	1801.6787.03
Memory upgrade, 400 Mpoints per channel	R&S®RTO6-B104	1801.6793.02
Memory upgrade, 1 Gpoint per channel	R&S®RTO6-B110	1801.6806.04
Bandwidth upgrades [17]		
Upgrade of the R&S®RTO6-B90 option to 1 GHz bandwidth	R&S®RTO6-B201	1801.7277.02
Upgrade of the R&S®RTO6-B90 option to 2 GHz bandwidth	R&S®RTO6-B202	1801.7283.02
Upgrade of the R&S®RTO6-B90 option to 3 GHz bandwidth	R&S®RTO6-B203	1801.7290.02
Upgrade of the R&S®RTO6-B90 option to 4 GHz bandwidth	R&S®RTO6-B204	1801.7302.02
Upgrade of the R&S®RTO6-B90 option to 6 GHz bandwidth	R&S®RTO6-B206	1801.7319.02
Upgrade of the R&S®RTO6-B91 option to 2 GHz bandwidth	R&S®RTO6-B212	1801.7325.02
Upgrade of the R&S®RTO6-B91 option to 3 GHz bandwidth	R&S®RTO6-B213	1801.7331.02
Upgrade of the R&S®RTO6-B91 option to 4 GHz bandwidth	R&S®RTO6-B214	1801.7348.02
Upgrade of the R&S®RTO6-B91 option to 6 GHz bandwidth	R&S®RTO6-B216	1801.7354.02
Upgrade of the R&S®RTO6-B92 option to 3 GHz bandwidth	R&S®RTO6-B223	1801.7360.02
Upgrade of the R&S®RTO6-B92 option to 4 GHz bandwidth	R&S®RTO6-B224	1801.7377.02
Upgrade of the R&S®RTO6-B92 option to 6 GHz bandwidth	R&S®RTO6-B226	1801.7383.02
Upgrade of the R&S®RTO6-B93 option to 4 GHz bandwidth	R&S®RTO6-B234	1801.7390.02
Upgrade of the R&S®RTO6-B93 option to 6 GHz bandwidth	R&S®RTO6-B236	1801.7402.02
Upgrade of the R&S®RTO6-B94 option to 6 GHz bandwidth	R&S®RTO6-B246	1801.7419.02
Software options		
Low speed serial buses triggering and decoding (I²C/SPI/UART/I²S/NRZ/Manchester)	R&S®RTO6-K510	1801.7019.02
Automotive protocols triggering and decoding (CAN/CAN FD/CAN XL/LIN/ FlexRay/SENT/CXPI)	R&S®RTO6-K520	1801.7025.02
Aerospace protocols triggering and decoding (MIL-STD-1553/ARINC 429/ SpaceWire)	R&S®RTO6-K530	1801.7031.02
Ethernet protocols triggering and decoding (10BASE-T/100BASE-TX/MDIO)	R&S®RTO6-K540	1801.7048.02
MIPI low speed triggering and decoding (RFFE/I³C)	R&S®RTO6-K550	1801.7054.02
Automotive Ethernet triggering and decoding (10BASE-T1S/100BASE-T1/ 1000BASE-T1)	R&S®RTO6-K560	1801.7060.02
USB protocols triggering and decoding (USB2.0/USB3.1/SSIC/USB PD)	R&S®RTO6-K570	1801.7077.02
MIPI high speed triggering and decoding (D-PHY/M-PHY)	R&S®RTO6-K580	1801.7083.02
PCI express triggering and decoding (8b10b/PCI1.0/2.0)	R&S®RTO6-K590	1801.7090.02
Triggering and decoding bundle	R&S®RTO6-TDBDL	1801.7725.02
Compliance tests (R&S®ScopeSuite based)		
USB 2.0 compliance test	R&S®RTO6-K21	1801.6912.02
Ethernet compliance test (10/100/1000BASE-T/EEE)	R&S®RTO6-K22	1801.6929.02
Ethernet compliance test (2.5/5/10GBASE-T)	R&S®RTO6-K23	1801.6935.02
Ethernet compliance test (100BASE-T1)	R&S®RTO6-K24	1801.6941.02

[17] Bandwidth upgrades up to 3 GHz bandwidth are performed by license keycode, bandwidth upgrades to 4 GHz and 6 GHz are performed at a Rohde & Schwarz service center, where the oscilloscope will also be calibrated.

Designation	Type	Order No.
MIPI D-PHY compliance test	R&S®RTO6-K26	1801.6958.02
MIPI D-PHY 2.5 compliance test	R&S®RTO6-K27	1803.6578.02
PCI Express 1.1/2.0 compliance test	R&S®RTO6-K81	1801.6964.02
Ethernet compliance test (1000BASE-T1)	R&S®RTO6-K87	1801.6970.02
Ethernet compliance test (MGBASE-T1)	R&S®RTO6-K88	1801.7890.02
Ethernet compliance test (10BASE-T1)	R&S®RTO6-K89	1801.6987.02
DDR3/DDR3L/LPDDR3 signal integrity debugging and compliance test	R&S®RTO6-K91	1801.6993.02
eMMC compliance test	R&S®RTO6-K92	1801.7160.02
R&S®ScopeSuite automation	R&S®RTO6-K99	1801.7690.02
Compliance tests (R&S®ScopeSuite+ based)		
R&S®ScopeSuite+ base option	R&S®SPLUS	1804.8774.02
R&S®ScopeSuite+ 100BASE-T1 automotive Ethernet compliance test	R&S®SPLUS-K24	1804.8774.02
R&S®ScopeSuite+ 1000BASE-T1 automotive Ethernet compliance test	R&S®SPLUS-K87	1804.8797.02
R&S®ScopeSuite+ 10BASE-T1S automotive Ethernet compliance test	R&S®SPLUS-K89	1804.8780.02
R&S®ScopeSuite+ Remote automation API	R&S®SPLUS-K99	1804.8945.02
Analysis		
I/Q software interface	R&S®RTO6-K11	1801.6812.02
Jitter analysis	R&S®RTO6-K12	1801.6829.02
Clock data recovery	R&S®RTO6-K13	1801.6835.02
Power analysis	R&S®RTO6-K31	1801.6858.02
Spectrogram	R&S®RTO6-K37	1801.6870.02
User-defined math	R&S®RTO6-K39	1803.6778.02
Deembedding base option	R&S®RTO6-K121	1801.6887.02
Embedding and equalization	R&S®RTO6-K126	1801.8109.02
Video raster analysis	R&S®RTO6-K129	1801.8609.02
TDR/TDT analysis	R&S®RTO6-K130	1801.6893.02
Advanced jitter analysis	R&S®RTO6-K133	1801.6906.02
Advanced jitter and noise analysis	R&S®RTO6-K134	1801.7677.02
PAM analysis	R&S®RTO6-K135	1801.8050.02
Advanced eye analysis	R&S®RTO6-K136	1801.8080.02
EMC/ESD test	R&S®RTO6-K155	1801.8696.02
Bus analysis	R&S®RTO6-K500	1801.6864.02
Health and utilization monitoring service (HUMS)	R&S®RTO6-K980	1801.8821.02
Windows 10-2021 upgrade (Windows 10 IOT ENT 2021 LTSC supports security updates until 2032)	R&S®RTO6-U1	1801.8744.02
Windows 11 upgrade (upgrade of R&S®RTO6 with Windows 10 operation system)	R&S®RTO6-U2	1801.8750.02
Probes		
500 MHz, passive, 10:1, 1 MΩ, 9.5 pF, max. 400 V	R&S®RT-ZP10	1409.7550.00
400 MHz, passive, high-voltage, 100:1, 50 MΩ, 7.5 pF, 1 kV (RMS)	R&S®RT-ZH10	1409.7720.02
400 MHz, passive, high-voltage, 1000:1, 50 MΩ, 7.5 pF, 1 kV (RMS)	R&S®RT-ZH11	1409.7737.02
8.0 GHz, passive, transmission line, 10:1, 500 Ω, 0.3 pF, 20 V (RMS)	R&S®RT-ZZ80	1409.7608.02
1.0 GHz, active, 1 MΩ || 0.8 pF	R&S®RT-ZS10E	1418.7007.02
1.0 GHz, active, 1 MΩ || 0.8 pF, R&S®ProbeMeter, micro button	R&S®RT-ZS10	1410.4080.02
1.5 GHz, active, 1 MΩ || 0.8 pF, R&S®ProbeMeter, micro button	R&S®RT-ZS20	1410.3502.02
3.0 GHz, active, 1 MΩ || 0.8 pF, R&S®ProbeMeter, micro button	R&S®RT-ZS30	1410.4309.02
6.0 GHz, active, 1 MΩ || 0.3 pF, R&S®ProbeMeter, micro button	R&S®RT-ZS60	1418.7307.02
1.5 GHz, active, differential, 1 MΩ || 0.6 pF, R&S®ProbeMeter, micro button	R&S®RT-ZD20	1410.4409.02
3.0 GHz, active, differential, 1 MΩ || 0.6 pF, R&S®ProbeMeter, micro button	R&S®RT-ZD30	1410.4609.02
4.5 GHz, active, differential, 1 MΩ || 0.4 pF, R&S®ProbeMeter, micro button	R&S®RT-ZD40	1410.5205.02
10 MHz, current, AC/DC, 0.01 V/A, 150 A (RMS)	R&S®RT-ZC10	1409.7750.02
100 MHz, current, AC/DC, 0.1 V/A, 30 A (RMS)	R&S®RT-ZC20	1409.7766.02
120 MHz, AC/DC, 1 V/A, 5 A (RMS)	R&S®RT-ZC30	1409.7772K02
2 MHz, current, AC/DC, 0.01 V/A, 500 A (RMS), Rohde & Schwarz probe interface	R&S®RT-ZC05B	1409.8204.02
10 MHz, current, AC/DC, 0.01 V/A, 150 A (RMS), Rohde & Schwarz probe interface	R&S®RT-ZC10B	1409.8210.02
50 MHz, AC/DC, 0.1 V/A, 30 A (RMS), Rohde & Schwarz probe interface	R&S®RT-ZC15B	1409.8227.02
100 MHz, current, AC/DC, 0.1 V/A, 30 A (RMS), Rohde & Schwarz probe interface	R&S®RT-ZC20B	1409.8233.02
Multichannel power probe, 2 × 4 voltage/current channels, for R&S®RTO6/R&S®RTE	R&S®RT-ZVC04	1326.0259.04
Multichannel power probe, 2 × 2 voltage/current channels, for R&S®RTO6/R&S®RTE	R&S®RT-ZVC02	1326.0259.02
Probe set for E and H near-field measurements, two passive E and three passive H near-field probes, 30 MHz to 3 GHz	R&S®HZ-15	1147.2736.02
Probe set for H near-field measurements, two passive H near-field probes, 30 MHz to 3 GHz	R&S®HZ-17	1339.4141.02
Probe accessories		
Accessory set, for R&S®RT-ZP10 passive probe (2.5 mm probe tip)	R&S®RT-ZA1	1409.7566.00
Spare accessory set, for R&S®RT-ZS10/-ZS10E/-ZS20/-ZS30	R&S®RT-ZA2	1416.0405.02

Designation	Type	Order No.
Pin set, for R&S®RT-ZS10/-ZS10E/-ZS20/-ZS30	R&S®RT-ZA3	1416.0411.02
Mini clips	R&S®RT-ZA4	1416.0428.02
Micro clips	R&S®RT-ZA5	1416.0434.02
Lead set	R&S®RT-ZA6	1416.0440.02
Pin set, for R&S®RT-ZD20/-ZD30	R&S®RT-ZA7	1417.0609.02
Pin set, for R&S®RT-ZD40	R&S®RT-ZA8	1417.0867.02
Probe box to N/USB adapter	R&S®RT-ZA9	1417.0909.02
Adapter SMA(f) to BNC(m)	R&S®RT-ZA10	1416.0457.02
Probe power supply	R&S®RT-ZA13	1409.7789.02
External attenuator, 10:1, 2.0 GHz, 70 V DC, 46 V AC (peak)	R&S®RT-ZA15	1410.4744.02
Extended cable set, for R&S®RT-ZVC, PCB probing, 1 current and voltage lead, length: 32 cm	R&S®RT-ZA30	1333.1686.02
Extended cable set, for R&S®RT-ZVC, 4 mm probing, 1 current and voltage lead, length: 32 cm	R&S®RT-ZA31	1333.1692.02
Oscilloscope interface cable, for R&S®RT-ZVC (included in R&S®RT-ZVC02/-ZVC04, 1326.0259.02/.04)	R&S®RT-ZA33	1333.1770.02
Extended cable set, for R&S®RT-ZVC, 4 mm probing, 1 current and voltage lead, length: 1 m	R&S®RT-ZA34	1333.1892.02
Extended cable set, for R&S®RT-ZVC, PCB probing, 1 current and voltage lead, length: 1 m	R&S®RT-ZA35	1333.1905.02
Solder-in cable set, for R&S®RT-ZVC, 4 current and voltage solder-in cables, solder-in pins	R&S®RT-ZA36	1333.1911.02
Extended cable set, for R&S®RT-ZVC, BNC connector, 1 current and voltage lead, length: 16 cm	R&S®RT-ZA37	1337.9130.02
Adapter, Rohde & Schwarz probe interface to 2.92 mm/3.5 mm/SMA, incl. USB-C port	R&S®RT-ZA50	1803.5265.02
Adapter, 2.92 mm/3.5 mm/SMA to Rohde & Schwarz probe interface, incl. USB-C port	R&S®RT-ZA51	1803.5365.02
Accessories		
Front cover, for R&S®RTO64 oscilloscopes	R&S®RTO6-Z1	1801.6641.02
Soft case, for R&S®RTO64 oscilloscopes and accessories	R&S®RTO6-Z3	1801.6658.02
Transit case, for R&S®RTO64/RTE oscilloscopes and accessories	R&S®RTO6-Z4	1801.6712.02
Probe pouch, for R&S®RTO64 oscilloscopes	R&S®RTO6-Z5	1317.7031.02
USB 2.0 compliance test fixture set	R&S®RT-ZF1	1317.3420.02
Ethernet compliance test fixture set	R&S®RT-ZF2	1317.5522.02
Ethernet 1000BASE-T1 jitter test cable	R&S®RT-ZF2C	1317.5639.02
Frequency converter (100BASE-T1)	R&S®RT-ZF3	5025.0670.02
Ethernet 10BASE-TE fixture	R&S®RT-ZF4	1333.0915.02
Ethernet probe fixture	R&S®RT-ZF5	1333.0938.02
Frequency converter (1000BASE-T1)	R&S®RT-ZF6	1337.8579.02
Automotive Ethernet trigger and decode fixture	R&S®RT-ZF7	1801.3688.02
SMA adapter	R&S®RT-ZF7A	1801.4126.02
SMA adapter for PoDL	R&S®RT-ZF7P	1802.9680.02
Test fixture 10BASE-T1S	R&S®RT-ZF7P	1802.9680.03
Automotive Ethernet compliance fixture	R&S®RT-ZF8	1801.3694.02
Probe deskew and calibration test fixture	R&S®RT-ZF20	1800.0004.02
3 GHz, 20 dB preamplifier, 100 V to 230 V power adapter, for R&S®HZ-15	R&S®HZ-16	1147.2720.02
19" rackmount kit for R&S®RTO64 oscilloscopes, 8 HU resulting height	R&S®ZZA-RTO6	1801.6729.02

Warranty and service

Warranty		
Base unit		1 year
All other items		1 year
Service options		
	Service plans	**On demand**
Calibration	up to five years [18]	pay per calibration
Warranty and repair	up to five years [18]	standard price repair
Contact your Rohde & Schwarz sales office for further details.		

[18] For extended periods, contact your Rohde & Schwarz sales office.

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