

Keysight Technologies Physical Layer Test System (PLTS) 2018

Data Collection & Analysis Software for Frequency and
Time Domain Data with Optional Instrument Control

Includes What's New in PLTS 2018 Software

Technical Overview



What's New with PLTS 2018?

Breakthrough spatial resolution of 6 picoseconds

The new Physical Layer Test System (PLTS) 2018 has significant breakthrough capabilities with regards to resolving adjacent impedance discontinuities within high-speed interconnects, such as cables, backplanes, PCBs and connectors. Many signal integrity laboratories around the world have benefited from the power of PLTS in the R&D prototype test phase. PLTS 2018 now supports the new N5291A PNA MM-wave system that provides a single continuous sweep of 900 Hz to 120 GHz in a single box (see Figure 1 below). This new hardware support enables not only excellent low frequency performance for power integrity applications, but also achieves the best-in-class highest stop frequency of 120 GHz which directly translates to a 6-picosecond equivalent system risetime. This 6-picosecond risetime allows adjacent impedance discontinuities of less than 400 microns to be resolved in high-performance BGA (ball grid array) ceramic IC packages. High-speed SERDES chipsets designed for 400G network and data centers can now be fully characterized and optimized for high performance.



Figure 1. The N5291A enables PLTS 2018 to achieve 6-picosecond equivalent system risetime measurements providing better than 400-micron spatial resolution.

Python interface

Another significant enhancement to PLTS 2018 is the addition of a Python programming interface. Python is a widely used high-level programming language that features a dynamic system that supports multiple programming paradigms, including object-oriented, imperative, functional programming, and procedural styles. While the previous version of PLTS 2017 used the MATLAB programming interface, Python allows for custom processing of data out of and back into PLTS. This new language interface furthers the remote and factory automation applications for high-volume production of backplanes, PCBs, connectors, cables and IC packages. See the PLTS 2018 built-in Help for additional details and programming examples.

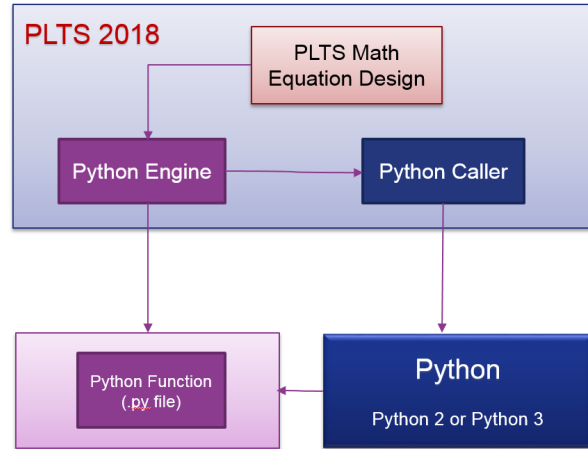


Figure 2. The new Python interface provides powerful automation of measurements for production environments.

64-port S-parameter analysis

The last major enhancement to PLTS 2018 is 64-port S-parameter capability. Many sophisticated backplane applications have multiple channels that need extensive crosstalk characterization in order to comply to the new high-speed digital standards. The 64-port S-parameter analysis allows eight differential pairs to be fully scrutinized for near-end and far-end crosstalk in any combination. This allows over 4096 waveforms to be recalled onto a PLTS canvas quickly and easily in multiple domains. There are very few signal integrity tools on the market that have a complete cross talk characterization of hardware and software built into a single analysis system.

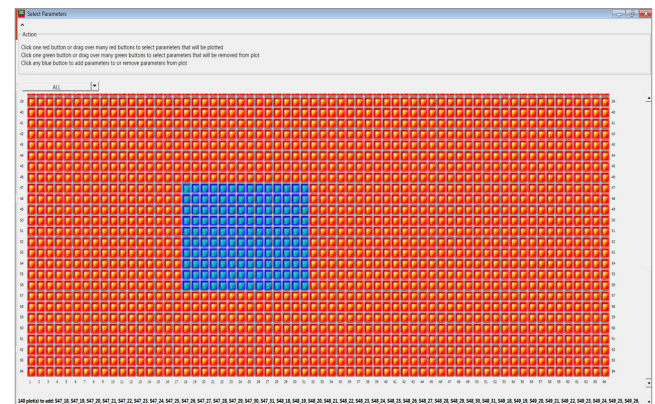


Figure 3. The 64-port S-parameter analysis capability in PLTS 2018 includes Automatic Fixture Removal (AFR), Round Robin, N-port Reference Plane Adjustment, Import, Export and more.

Many other features not mentioned in this document can be found in PLTS 2018. Our design team looks forward to working together with you to overcome any signal integrity problems and help you design the highest quality data transmission channels possible.

Why is Physical Layer Testing Required?

The next generation computer and communication systems now being developed will handle data rates of multiple gigabits/second. Many systems will incorporate processors and SERDES chip sets that exceed GigaHertz clock frequencies. New and troubling input/output issues are emerging as switches, routers, server blades, and storage area networking equipment moving toward 100 Gbps data rates. Digital design engineers choosing chip-to-chip and backplane technologies for these systems are finding signal integrity challenges that have not been encountered before.

Traditional parallel bus topologies are running out of bandwidth. As parallel busses become wider, the complexity and cost to route on PC boards increase dramatically. The growing skew between data and clock lines has become increasingly difficult to resolve within parallel busses. The solution is fast serial channels. The newer serial bus structure is quickly replacing the parallel bus structure for high-speed digital systems. Engineers have been turning to a multitude of gigabit serial interconnect protocols with embedded clocking to achieve the goal of simple routing and more bandwidth per pin. However, these serial interconnects bring their own set of problems.

In order to maintain the same total bandwidth as the older parallel bus, the new serial bus needs to increase its data rate. As the data rate increases through serial interconnects, the rise time of the data transition from a zero logic level to a one logic level becomes shorter. This shorter rise time creates larger reflections at impedance discontinuities and degrade the eye diagram at the end of the channel. As a result, physical layer components such as printed circuit board traces, connectors, cables, and IC packages can no longer be ignored. In fact, in many cases, the silicon is so fast that the physical layer device has become the bottleneck.

In order to maintain signal integrity throughout the complete channel, engineers are moving away from single-ended circuits and now use differential circuits. The differential circuit provides good Common Mode Rejection Ratio (CMRR) and helps shield adjacent PCB traces from crosstalk. Properly designed differential transmission lines will minimize the undesirable effect of mode conversion and enhance the maximum data rate throughput possible. Unfortunately, differential signaling technology is not always an intuitive science.

Differential transmission lines coupled with the microwave effects of high-speed data have created the need for new design and validation tools for the digital design engineer. Understanding the fundamental properties of signal propagation through measurement and post-measurement analysis is mandatory for today's leading edge telecommunication and computer systems. The traditional Time Domain Reflectometer (TDR) is still a very useful tool, but many times the Vector Network Analyzer (VNA) is needed for the complete characterization of physical layer components. There is a strong need for a test and measurement system that will allow simple characterization of complex microwave behavior seen in high speed digital interconnects. In fact, many digital standards groups have now recognized the importance of specifying frequency domain physical layer measurements as a compliance requirement. Many standards including Serial ATA and PCI Express® have adopted the SDD21 parameter (input differential insertion loss) as a required measurement to ensure channel compliance. This parameter is an indication of the frequency response that the differential signal sees as it propagates through the high-speed serial channel. An example of a proposed SDD21 compliance mask is shown in Figure 4 for the Channel Electrical Interface (CEI) working group for the Optical Internetworking Forum (OIF).

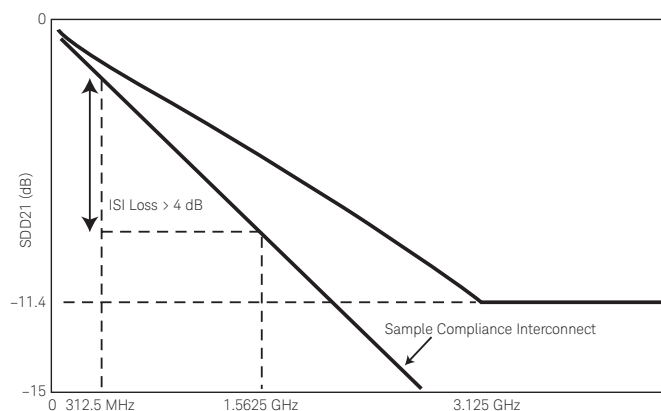


Figure 4. Today's digital standards are now using frequency domain measurements for compliance testing, such as this input differential insertion loss (SDD21) mask for XAUI.

Why is Physical Layer Testing Required? (continued)

A single test system can provide the total view

As the combination of both time-domain and frequency domain analysis becomes more important, the need for multiple test systems becomes difficult to manage. A single test system that can fully characterize differential high-speed digital devices, while leaving domain and format of the analysis up to the designer, is a very powerful tool. Keysight's Physical Layer Test System (PLTS) is designed specifically for this purpose.

PLTS has been designed specifically for signal integrity analysis. PLTS software guides the user through hardware setup and calibration, and controls the data acquisition. It automatically applies patented transformation algorithms to present the data in both frequency and time domains, in both forward and reverse transmission and reflection terms, and in all possible modes of operation (single-ended, differential, and mode-conversion).

A powerful virtual bit pattern generator feature allows a user-defined binary sequence to be applied to the measured data to convolve eye pattern diagrams. Next, highly accurate RLCG¹ models can be extracted and used to enhance the accuracy of your models and simulations.

PLTS provides design confidence through complete characterization

Physical-layer structures have increasingly become the bottleneck in high-speed digital system performance. At low data rates, these interconnects are electrically short. The driver and receiver are typically the biggest contributors to signal integrity. But as clock speeds, bus speeds, and link speeds all push past the gigabit-per-second mark, physical layer characterization becomes more critical.

Another challenge for today's digital designers is the trend to differential topologies. Fully understanding device performance requires analysis in all possible modes of operation.

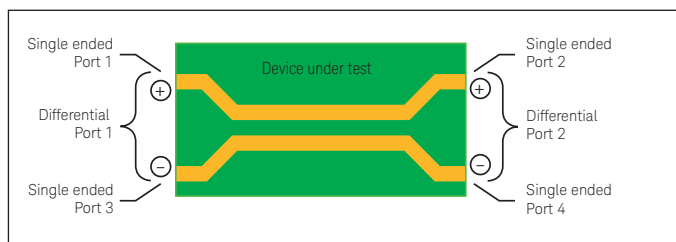


Figure 5. A differential structure operates in many modes. Single-ended analysis can reveal sources of asymmetry on this differential transmission line.

Time-domain analysis is typically used for characterization of these physical-layer structures, but often, the designer concentrates only on the intended modes of operation. For a complete time-domain view, step and impulse responses in reflection and transmission (TDR and TDT) must be seen. The analysis must include the unintended modes of operation as well.

Frequency-domain analysis, again in all possible modes of operation, is also necessary for fully characterizing these physical-layer structures. The s-parameter model describes the analog behavior exhibited by these digital structures. This behavior includes reflections from discontinuities, frequency dependent losses, crosstalk, and EMI performance.

For translating device performance into standards compliance, eye diagrams add an important statistical analysis. And for leveraging this complete characterization into improved simulations, measurement-based s-parameter or RLCG model extraction completes the picture.

Mode	Time domain		Frequency domain	
	TDR	TDT	Reflection	Transmission
Differential	TDD11	TDD21	SDD11	SDD21
	TDD22	TDD12	SDD22	SDD12
Diff-to-comm	TCD11	TCD21	SCD11	SCD21
	TCD22	TCD12	SCD22	SCD12
Comm-to-diff	TDC11	TDC21	SDC11	SDC21
	TDC22	TDC12	SDC22	SDC12
Common	TCC11	TCC21	SCC11	SCC21
	TCC22	TCC12	SCC22	SCC12
Single-ended	T11	T21 T31 T41	S11	S21 S31 S41
	T22	T12 T32 T42	S22	S12 S32 S42
	T33	T13 T23 T43	S33	S13 S23 S43
	T44	T14 T24 T34	S44	S14 S24 S34

Figure 6. Complete characterization includes forward and reverse transmission and reflection, in all possible modes of operation, in both frequency and time domains.

1. An RLCG equivalent circuit model, also known as Telegrapher's Parameters, describes the electrical behavior of a passive transmission line. The model is a distributed network consisting of series resistance and inductance (R and L) and parallel capacitance and conductance (C and G).

Why is Physical Layer Testing Required? (continued)

PLTS enables mode-conversion analysis for early insight into EMI problems

The benefits of differential signaling include lower voltage swings, immunity from power supply noise, a reduced dependency on RF ground, and improved EMI performance (reduced generation and susceptibility). The extent to which a device can take advantage of these benefits is directly related to device symmetry.

Symmetric devices only respond to, and only generate, differential signals. These ideal devices do not respond to or generate common-mode signals, and they reject radiated external signals (i.e., power supply noise, harmonics of digital clocks or data, and EMI from other RF circuitry).

Asymmetric devices however, do not exhibit these benefits. When stimulated differentially, an asymmetric device will produce a common-mode response in addition to the intended differential response, and cause EMI radiation. Conversely, with a common-mode stimulus, an asymmetric device will produce an unintended differential response. This mode conversion is a source of EMI susceptibility.

Mode-conversion analysis is an important tool for understanding and improving device symmetry, and provides the designer with early insight to identify and resolve EMI problems at the design stage (Figure 7).

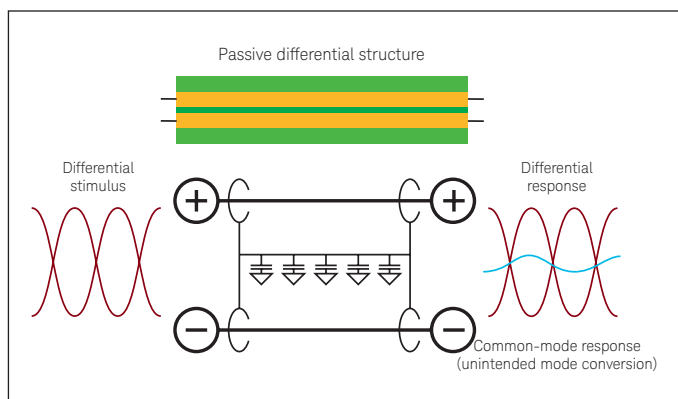


Figure 7. Asymmetric devices cause mode-conversions, which are indicators of EMI generation and susceptibility.

Mode conversion

A practical application of how mode conversion helps identify problems in physical layer devices is shown in Figure 8. This shows a XAUI backplane with two daughter cards that typically transmit data at 3.125 Gbps. The design objective for this high-speed differential channel is to minimize the crosstalk between adjacent differential PCB traces throughout the length of the channel. The channel consists of the linear passive combination of the backplane and two daughter cards. Any mode conversion from differential mode to common mode will generate EMI and create crosstalk that will be incident upon other channels and will degrade performance. However, locating the exact structure within the channel that creates the most mode conversion is not simple.

Looking at figure 8, the differential to common mode conversion time domain reflection parameter (TCD11) is time aligned with the differential impedance profile of the channel (TDD11) below it. A marker is placed on the largest magnitude peak of TCD11. This is where the physical structure within the channel is creating the most mode conversion and thus the source of the most crosstalk. We can align the TDD11 to the TCD11 in time and therefore co-locate the problematic structure on TDD11. To relate this structure to the channel, we use the differential impedance profile as a reference. From previous analysis, we know that the two capacitive discontinuities on TDD11 are the daughter card via field and motherboard via field, respectively. Since the marker falls upon the second discontinuity on TDD11, it is deduced that the motherboard via field is the biggest culprit to causing crosstalk in adjacent channels. This shows how identifying the mode conversion in a channel can be intuitive with proper analysis.

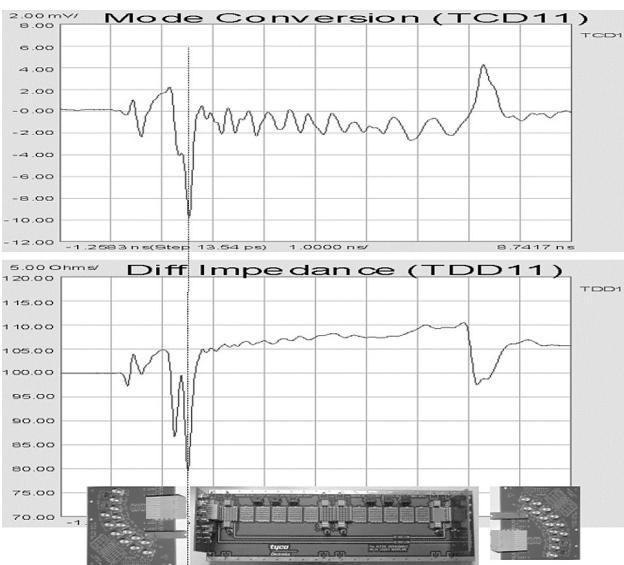


Figure 8. By aligning the impedance profile with the mode conversion profile, PLTS allows the pinpointing of crosstalk-generating structures within physical layer devices.

Why is Physical Layer Testing Required? (continued)

Remove unwanted effects from the measurement

Error correction

Over the years, many different approaches have been developed for removing the effects of the test fixture from the measurement (shown in Figure 9). The level of difficulty for each error correction technique is linearly related to the accuracy of each method. Time domain gating is perhaps the simplest and most straightforward method, but it is also the least accurate. Likewise, de-embedding is the most complicated method, but it is the most accurate. It is important to have a test system that will allow flexibility of choosing the method of error correction desired for each application.

Error correction techniques fall into two fundamental categories: direct measurement (pre-measurement processing) and de-embedding (post-measurement processing). Direct measurement requires specialized calibration standards that are connected to the end of a coaxial test cable and measured. The accuracy of the device measurement relies on the quality of these physical standards. De-embedding uses a model of the test fixture and mathematically removes the fixture characteristics from the overall measurement. This fixture de-embedding procedure can produce very accurate results.

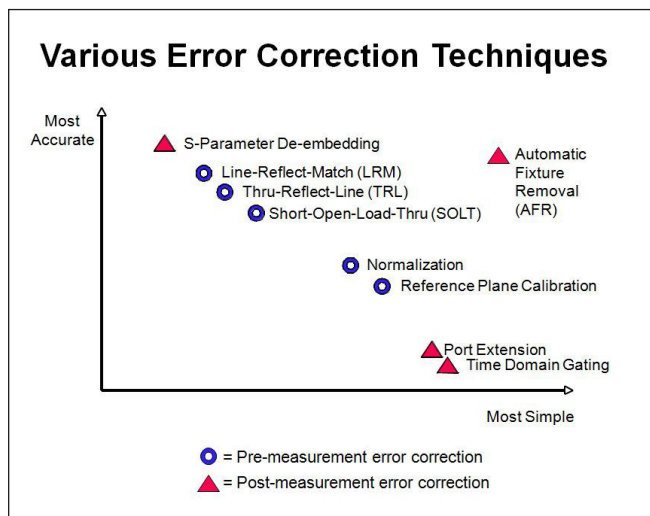


Figure 9. PLTS has advanced error correction techniques to allow flexibility for many applications.

Port Extension (also known as Phase Rotation) mathematically extends the calibration reference plane to the DUT.

This technique is easy to use, but assumes the fixture – the unwanted structure – looks like a perfect transmission line: a flat magnitude response, a linear phase response, and constant impedance. If the fixture is very well designed, this technique can provide good results.

Because gating essentially considers the magnitude of the unwanted discontinuity, and Port Extensions consider phase (electrical length), using the two tools together may provide optimum results.

Time-domain gating (Figure 10) is similar to port extension, in that it is also very easy and fast. The user simply defines two points in time or distance, and the software mathematically replaces the actual measured data in that section with data representing an "ideal" transmission line. The return loss is then recalculated to show the effects of the change in the frequency domain.

One practical application of time-domain gating is as a confidence check before replacing a suspect connector.

Figure 10 illustrates how this technique might be used.

De-embedding (Figure 11) uses an accurate linear model of the fixture, or measured s-parameter data of the fixture. This fixture data can then be removed mathematically from the DUT measurement data in post-processing.

Calibration at the DUT reference plane has the advantage that the precise characteristics of the fixture do not need to be known beforehand, as they are measured and corrected for during the calibration process.

An example of this technique is microprobing using a calibration substrate, where the calibration reference plane is established at the probe tips, rather than at the end of the coaxial test cables.

Advanced calibration techniques (TRL/LRM) – originally developed for wafer probing applications – provide additional options.

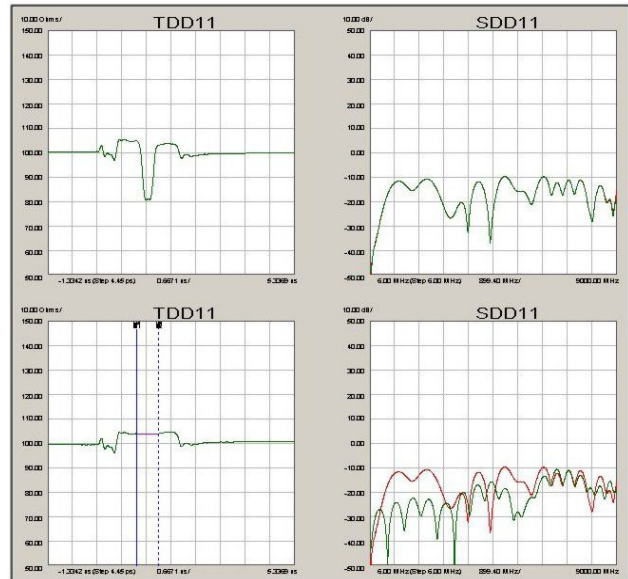


Figure 10. In this rather extreme example of time-domain gating, the top plots show the measured differential step impedance and return loss. The lower left plot shows a gate added to remove the large discontinuity in the center of the trace. On the lower right, the measured and the recalculated return losses are displayed. In this case, the gate improved the return loss by more than 10 dB within the frequency band of interest.

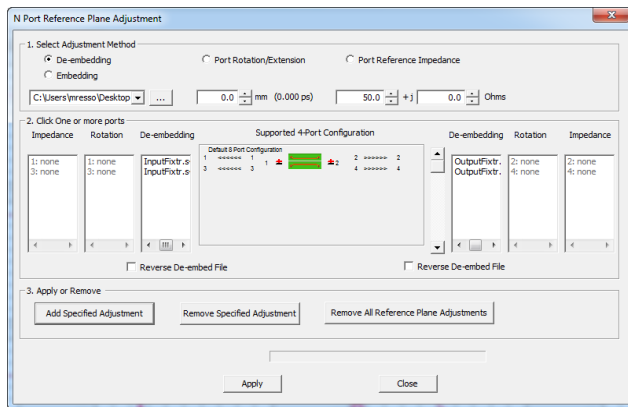


Figure 11. The effects of test fixtures can be removed from the device in post-processing through de-embedding.

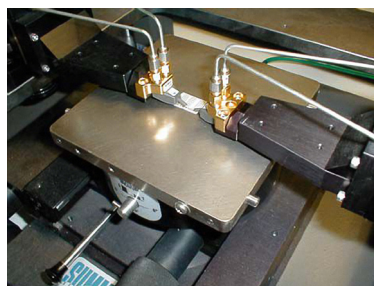


Figure 12. A microprobing application, where the calibration is performed using an impedance standard substrate, establishes the calibration reference plane at the probe tips.

PLTS Support for Microprobing Applications

Keysight works closely with leading microprobe and probe station suppliers to provide the best complete system solutions possible.

One of the most significant measurement challenges is connectivity. Test equipment provides a controlled coaxial environment, but what if the DUT – the backplane, the interface connector, the IC package – is non-coaxial?

Test fixtures can provide the required connectivity, but at a cost. The quality of the test fixture – its connectors, impedance discontinuities, parasitics, and dielectric losses – all contribute to less than ideal performance of the fixture. Subsequently, the accuracy of the device measurement is degraded.

Several techniques are available to remove these fixture effects (see Remove Unwanted Effects from the Measurement on page 6), but the accuracy of these techniques is greatly impacted by the quality of the fixture itself, or the availability of an accurate s-parameter model of the fixture (used for de-embedding). Microprobing can offer the user the ability to forego the test fixture and launch the stimulus directly at the device input. The response can be measured directly at the device output. Additionally, when calibration substrates are available, calibration can be performed directly at the probe tips. This achieves co-location of the calibration reference plane with the device measurement reference plane.

PLTS has the flexibility to accommodate many microprobe configurations. By adding the calibration substrate coefficients as a calibration kit, the process becomes as straightforward as a coaxial calibration.

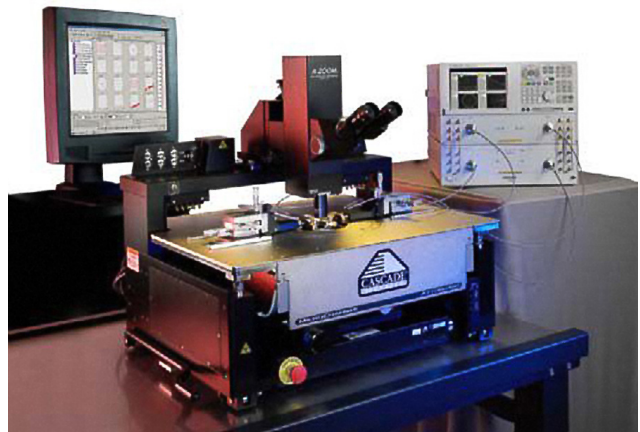


Figure 13. Cascade Microtech's Summit probe station.

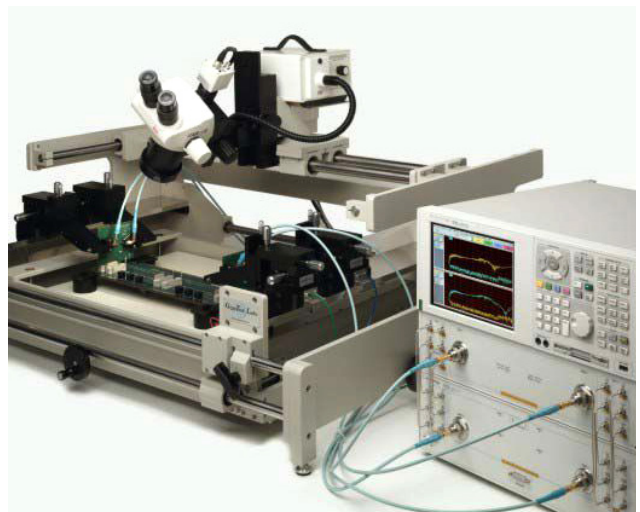


Figure 14. GigaTest Lab's GTL-4060 probe station.

PLTS Simplifies the Measurement Process

Device characterization with PLTS software is straightforward. The user interface has been designed to make setup, calibration, and measurement intuitive and error-free. A wizard guides the user through all of the required steps. The last prompt is to connect the device-under-test and initiate the measurement. Setup and calibration differs slightly between TDR-based and VNA-based systems. However, in both cases the PLTS software provides an intuitive wizard to assist in the step-by-step process.

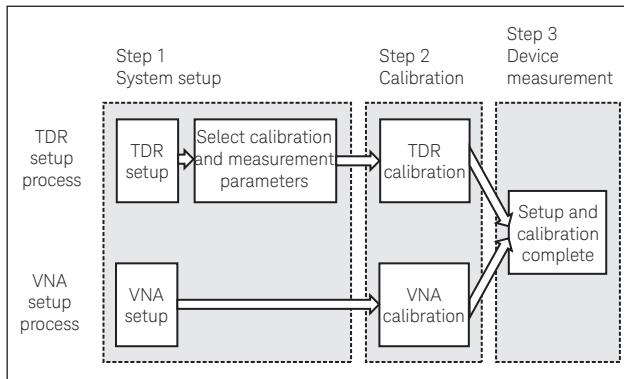


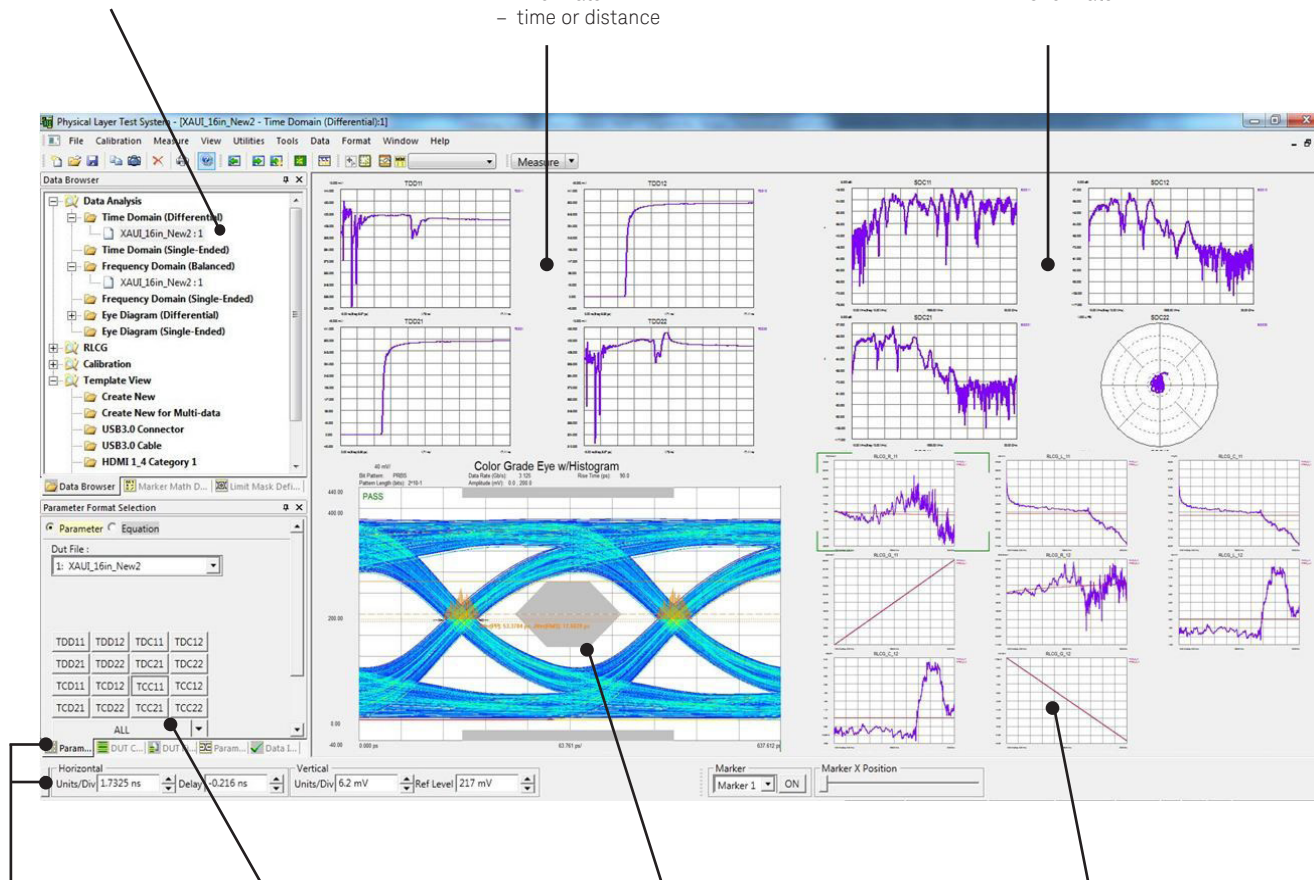
Figure 15. PLTS has a three-step system set up to make measurements intuitive and error-free.

Data analysis with n-port PLTS

File and view management with the data browser

Time domain analysis:
 - $2n^2$ parameters
 - 7 formats
 - time or distance

Frequency domain analysis:
 - $2n^2$ parameters
 - 8 formats



Format, scaling, and marker control with easy access toolbars

Plot and trace management with context-sensitive parameter buttons

Eye diagram analysis:
 - n^2 parameters
 - 8 formats

RLCG model extraction
 - $2n^2$ parameters

PLTS Simplifies the Measurement Process (continued)

Data analysis

All supported analysis types and formats are available immediately after the measurement is completed, and at any time thereafter. PLTS flexibility allows the user to begin where they are most familiar.

Time-domain analysis

The mixed-mode time domain is a common starting point. Initially, sixteen parameters are displayed in thumbnail view as shown below. These thumbnails represent four modes of device operation: differential, common-mode, and the two mode-conversion types (common-mode stimulus with differential response and differential stimulus with common-mode response). A double mouse-click on any of these thumbnails will expand the selected parameter to full screen for closer analysis.

Not shown here are the additional sixteen single-ended time-domain parameters.

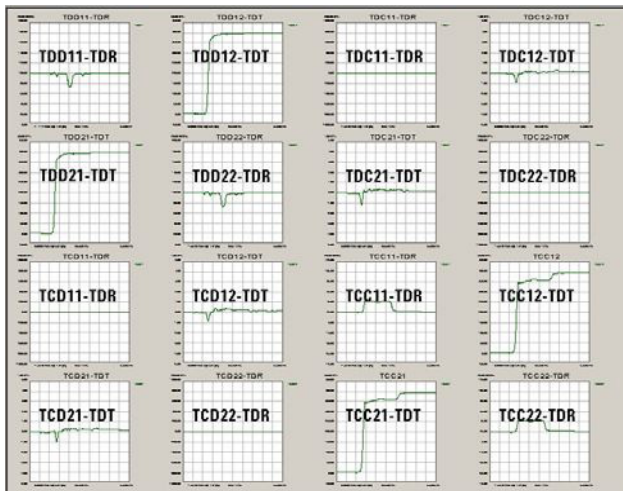


Figure 16. The mixed-mode time-domain matrix.

Frequency-domain analysis

The mixed-mode frequency domain is another common starting point.

Initially, sixteen parameters are displayed in thumbnail view as shown below. These thumbnails represent four modes of device operation: differential, common-mode, and the two mode-conversion types (common-mode stimulus with differential response and differential stimulus with common-mode response). A double mouse-click on any of these thumbnails will expand the selected parameter to full screen for closer analysis.

Not shown here are the additional sixteen single-ended frequency-domain parameters.

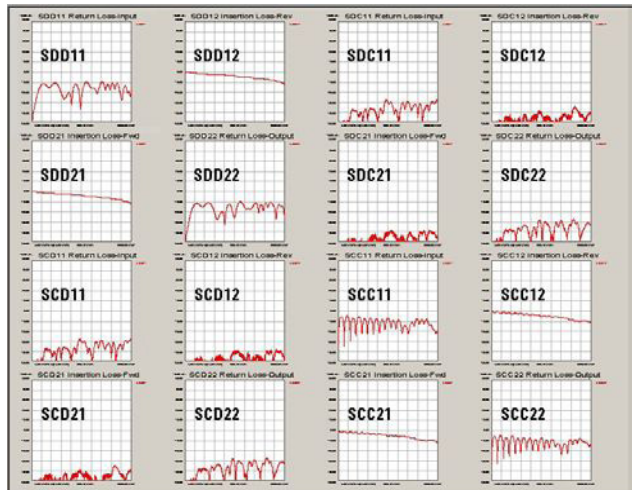


Figure 17. The mixed-mode frequency-domain matrix.

PLTS Simplifies the Measurement Process (continued)

Measurement-based eye diagram analysis

Using the built-in digital pattern generator, the user is able to define virtual bit pattern (as wide as $2^{32}-1$ bits). PLTS then convolves the selected bit pattern with the device impulse response to create an extremely accurate measurement-based eye pattern diagram.

This eliminates the need for a hardware pulse/pattern generator, and its flexibility allows for a great deal of "What if..." analysis.

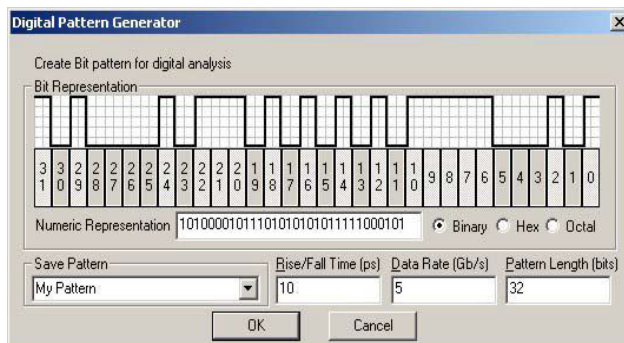


Figure 18. The digital pattern generator.

After the eye pattern is generated, marker functions can be used to make typical measurements like jitter, eye opening, rise and fall times, and more.

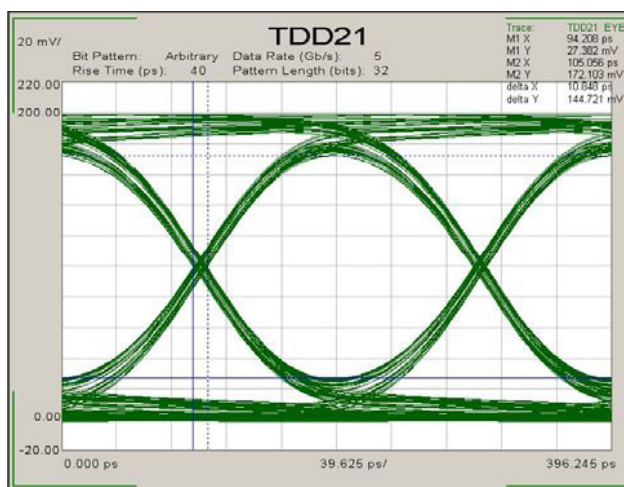


Figure 19. Eye pattern diagram.

PLTS Simplifies the Measurement Process (continued)

Multi-channel Simulation

The standard PLTS eye diagram is using an ideal data source (no jitter, no noise) to simulate the overlapped waveform data of the NRZ (non-return-zero) signals like PRBS transmitted through the measured backplane channel. To add advanced eye diagram capabilities, PLTS has a powerful feature to modify the Tx (transmitter) and Rx (receiver), and to add Xtalk (crosstalk) effects to simulate real world applications. This multi-channel simulation can quickly and efficiently simulate the following conditions:

- Specify bit pattern settings for data sources (either Tx or Xtalk)
- Add jitter to the data sources, the jitter includes RJ (random jitter), PJ (periodic jitter) and ISI (inter-symbol interference or so-called dirac jitter)

- Add source noise by specifying SNR (signal-to-noise ratio per symbol, or EsNodB).
- Add source equalization (the same meaning with pre-emphasis/de-emphasis).
- Add Rx linear equalization (adaptive or specify the taps manually).
- Add Xtalk effects from sources on other ports.

PLTS uses MATLAB to add jitter, noise, Tx and Rx equalization. PLTS invokes MATLAB in the background for doing the multi-channel eye simulation. For this feature, only the MATLAB Compiler Runtime (MCR) needs to be installed, and that has been included in PLTS install package.

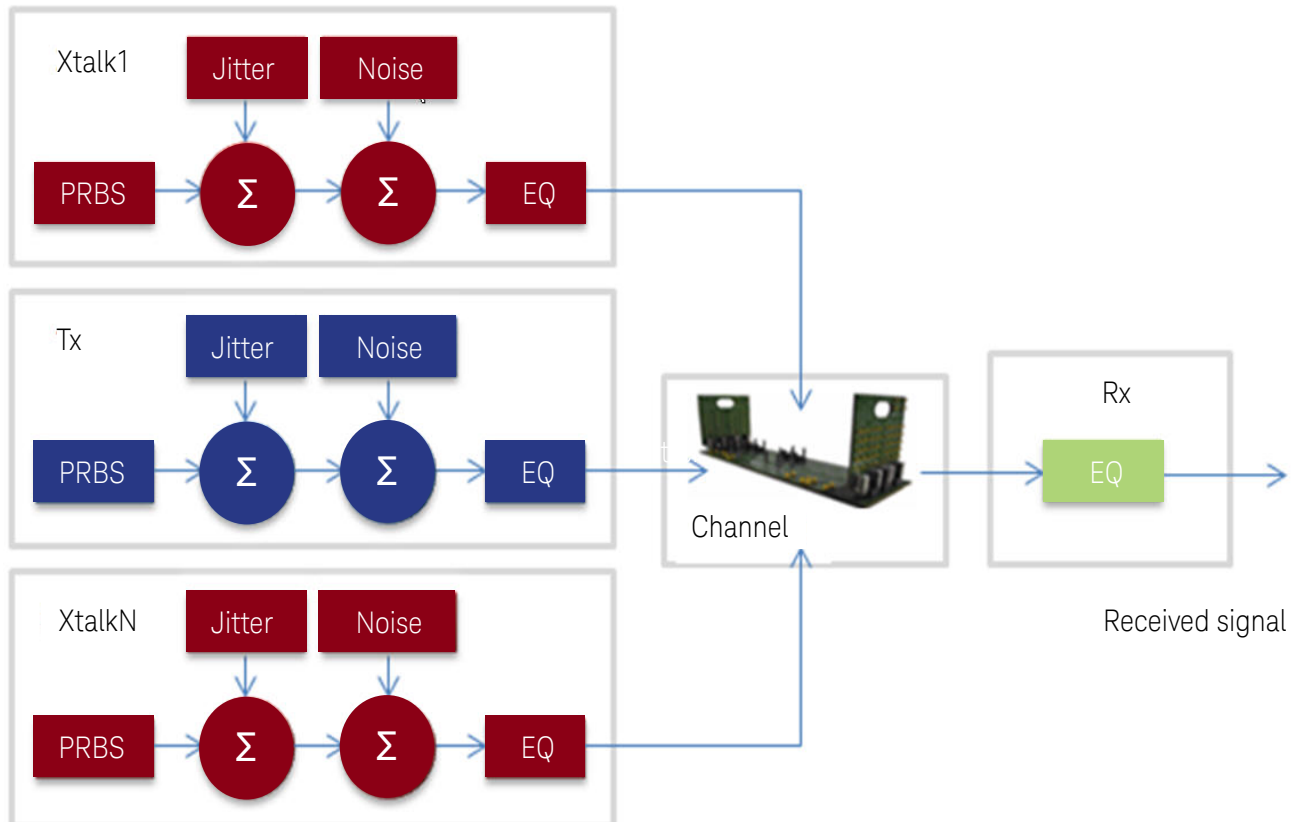


Figure 20. Multi-Channel Simulation is a fast and simple simulation engine specifically designed for high speed digital interconnect channels. It allows quick results with a minimal learning curve, yet provides powerful capabilities with full transmitter and receiver customization. Even IBIS-AMI models of transmitters and receivers are utilized for application specific chipset analysis.

PLTS Simplifies the Measurement Process (continued)

1. Detailed functionalities

Open or import a data set ([DEMO] E8364B 12-port 10 MHz-20 GHz. dut for example) and view the data in freq domain single-ended analysis mode, then go to the eye diagram view (either differential or single-ended). Now the menu of <Tools>-><Multi-channel Eye Diagram> is enabled.

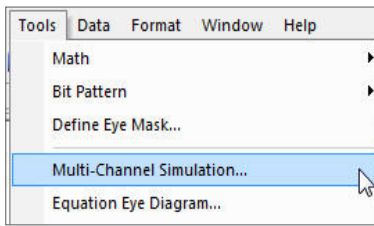


Figure 21. To activate Multi-Channel Simulation mode, select it from the Tools Menu

Click on the menu and the window below pops up:

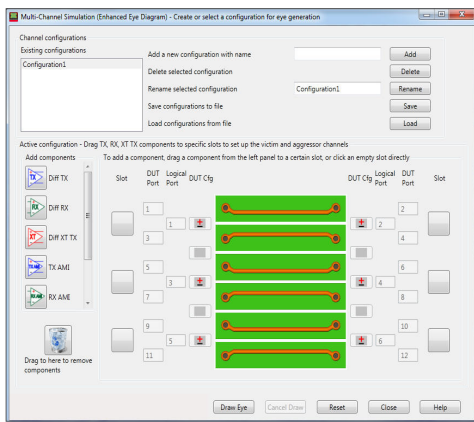


Figure 22. Main dialog box for Multi-Channel Simulation mode

Multi-channel eye diagram configuration: including the DUT configuration and the channel setup. The channel setup includes the information on which ports the Tx, Rx and Xtalks are added and the detailed settings of the Tx, Rx and Xtalks.

The multi-channel eye diagram configuration is dependent on a specific DUT configuration, if you select another data set with a different DUT configuration, this window will automatically update the multi-channel eye diagram configurations that match the current DUT configuration in the list. This also means you can use one configuration to simulate the eye diagrams of many data sets with the same DUT configuration.

From the Buttons you can Add, Delete, Rename, Save, Load configurations

1.1 Channel setup

The simulation channels can be set up by dragging Tx, Rx and Xtalk components to specific slots. To start the simulation, there must be

one Tx, one Rx, 0~N Xtalks. In the configuration below, a transmission channel of SDD43 and two Xtalk channels of SDD41 and SDD45 were set up.

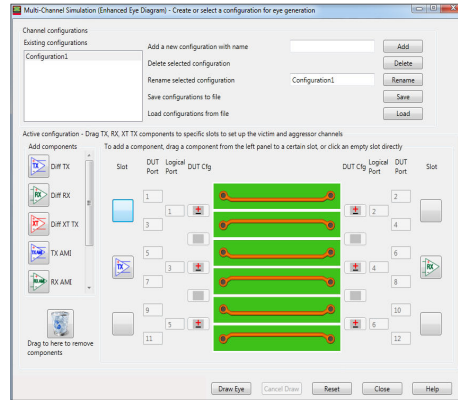


Figure 23. Near-end and far-end crosstalk simulation is simple and fast

1.2 Tx Settings

Click on the added Tx module (blue button) or right-click on it and select "Edit", one can change the Tx settings.

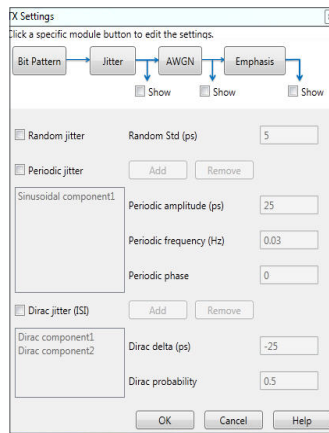


Figure 24. Transmitter and Receiver settings can be edited for pre-emphasis, jitter injection, noise injection, and multitude of equalization types.

- Ports - specify which port this module is added on. If you change the port number, the module will be moved to the new port specified.
- Pattern - bit pattern settings.
- Jitter - timing jitter is defined as the deviation of a signal's timing clock from the ideal clock. Timing jitter can be divided into two main subcategories: deterministic and random jitter.
- Equalization - in serial data transmission, pre-emphasis/de-emphasis is often used to compensate for losses over the channel which is larger at higher frequencies. The high frequency content is emphasized compared to the low frequency content which is de-emphasized. This is a form of transmitter equalization.

PLTS Simplifies the Measurement Process (continued)

RLCG model extraction

RLCG (resistance, inductance, capacitance, and conductance) models describe the electrical behavior of passive transmission lines in an equivalent circuit model.

From the measured S-parameters of a device, PLTS calculates the R, L, C, G, complex propagation constant, and complex characteristic impedance.

This provides a highly accurate, measurement-based coupled transmission line model for export into modeling and simulation software such as Keysight ADS, Synopsis HSPICE, and others.

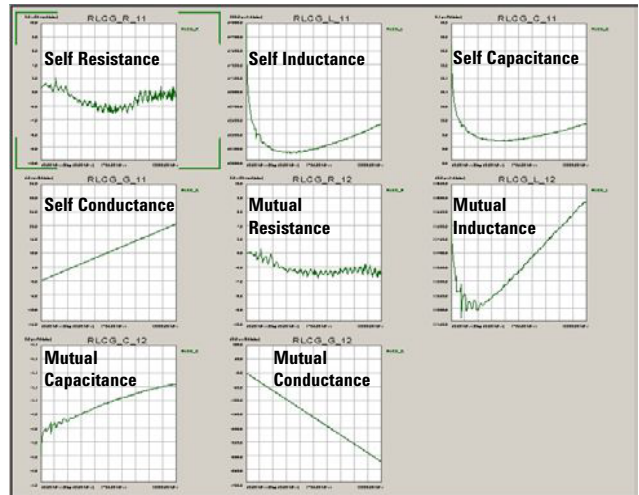
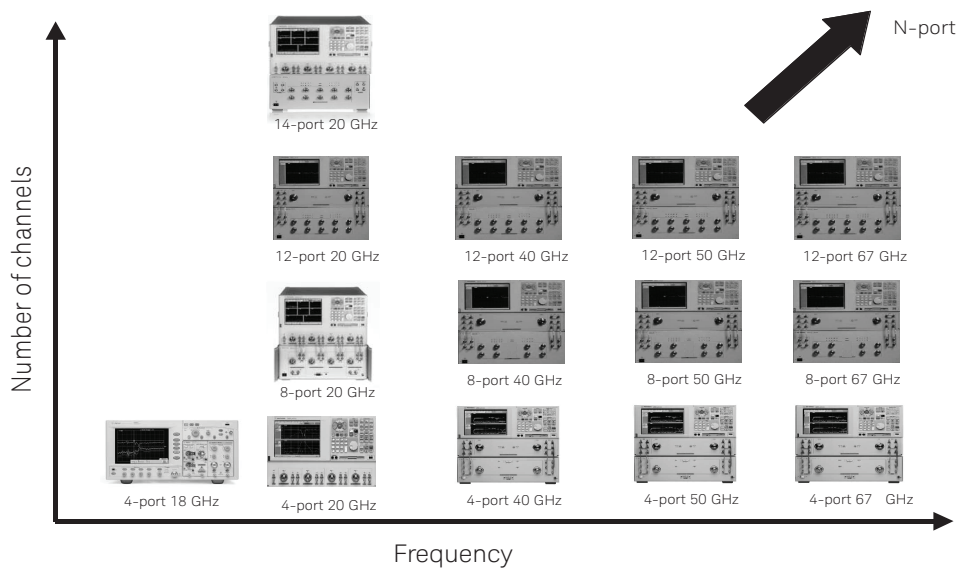


Figure 25. RLCG model extraction (W-Element shown).

PLTS Signal Integrity Solutions Portfolio



For all hardware configurations see PNA Family Microwave Network Analyzers Configuration Guide, part number 5992-1465EN.

PLTS Ordering Guide

PLTS system requirements

To ensure that PLTS operates effectively, your PC should have the following minimum requirements:

	Measurement mode ONLY	Off-line analysis mode
	In the lab, controlling test equipment and making quick analysis of the results.	In your office, performing “What if...” analysis, characterization, cross-domain analysis, filtering, waveform math, and eye diagram simulation.
CPU	1.5 GHz Quad-core	1.5 GHz Quad-core
Main memory (RAM)	4 GB	4+ GB
Virtual memory - As a general rule, virtual memory should be 1.5 to 2 times the size of main memory.	6 GB	6 GB
GPIB interface With PLTS 4.2, PLTS can connect to a PNA over LAN	Keysight 82357B USB/GPIB Interface for Windows or supported GPIB card (any National Instruments or Keysight 82340/41 or 82350 GPIB card)	No GPIB connection is required to use PLTS off-line. Saved (stored) measurement files can be recalled at any time for analysis.
Operating systems	Windows 7, 8.1 and 10	Windows 7, 8.1 and 10
Screen resolution	1280 x 1024 or greater required	1280 x 1024 or greater required
Display colors	High Color (16 Bit) or greater	High Color (16 Bit) or greater

PNA support²

The following Keysight vector network analyzers are supported by PLTS 2018. Firmware selection may depend on CPU and model number:
(<http://na.support.keysight.com/pna/cputype.html>)

- All PNA (N522xA/B) Series
- All PNA-X (N524xA/B) Series
- All PNA MM-Wave (N5290/91A)

The table below was current as of Jan. 8, 2018. For the most up-to-date recommended firmware, please go to the Keysight PNA Firmware Support website at <http://na.support.keysight.com/pna/firmware/firmware.htm>

PNA Model Numbers	Latest Production Releases ¹	Latest Customer Releases ² Recommended!	Notes
All PNA B Models (12.4" Display) • All N524B models • All N522B models • N5234B models • N5264B <small>Note: Minimum FW is A.12.70.06</small>	A.12.70.06 <small>(26 Jun 2017)</small>	A.12.85.04 <small>(06 Nov 2017)</small>	Release Notes
All Windows 7 PNAs ("A" Models) • All N524A models • All N522A models • N5231A to N5239A models • N5264A <small>Note: Min. Windows 7 FW is A.10.00.00 <small>Note: Min. FW for N5231A-N5239A is FW 029 and serial prefix of 40541 or higher is A.10.47.03</small></small>	A.10.47.06 <small>(02 Jun 2016)</small>	A.10.60.07 <small>(01 Dec 2017)</small>	Release Notes
All XP PNAs with large (10.4") display • N5242A - (Important! See Troubleshooting Note) • N5241A, N5244A, N5245A, N5247A, N5264A • N5231A, N5232A, N5234A, N5235A, N5239A • N5221A, N5222A, N5224A, N5225A, N5227A <small>Note: Above N5231A models require 0.05 or above. <small>Note: Above N5231A models require 0.40 or above.</small></small>	A.09.80.20 <small>(29 Mar 2015) (Not for sale with Option 029)</small>	A.09.90.19 <small>(23 Oct 2015)</small>	Release Notes
All PNA C Models • E8361C, E8362C, E8363C, E8364C, N5290C	A.09.33.09 <small>(19 May 2011)</small>	A.09.42.22 <small>(12 Dec 2015)</small>	Release Notes
All below models with 1.1 GHz CPU: • E8361A, E8362B, E8363B, E8364B, N5220A, 98239B ³ <small>For other models, see Supported Models Note below</small>	A.07.50.48 <small>(13 Mar 2009)</small>	A.07.50.67 <small>(19 Dec 2011) Also see Supported Models Note below</small>	Release Notes

ENA-PLTS Compatibility Guide

The ENA family of 4-port vector network analyzers is partially supported by PLTS 2018 software. The 4-port ENA family can be controlled, calibrated and measured remotely from PLTS software running on an external laptop. All the standard post-processing capability is available such as multi-domain analysis. However, there are some limitations. See list below.

1. The ENA family of VNAs targets manufacturing applications and is therefore not as flexible as the PNA family of VNAs using PLTS.
2. PLTS 2018 does not support ENA measurement collection through Option 5 (advanced calibration with Automatic Fixture Removal). However, AFR can be accomplished with the ENA family if the user imports the S-parameter data in manually. This support strategy is similar to the 86100 DCA's limitations with PLTS.
3. The ENA family does not support N-port calibration through PLTS software.
4. PLTS requires that the ENA have firmware A.08.00 or higher.

PLTS software ordering information

Model	Description
N1930B-1NP	Base analysis networkable license; 1-year update subscription
N1930B-1FP	Base analysis fixed license; 1-year update subscription
N1930B-1TP	Base analysis transportable license (USB Key); 1-year update subscription
N1930B-3NP	Measurement & cal networkable license; 1-year update subscription
N1930B-3FP	Measurement & cal fixed license; 1-year update subscription
N1930B-3TP	Measurement & cal transportable license (USB Key); 1-year update subscription
N1930B-5NP	Advanced calibration networkable license; 1-year update subscription
N1930B-5FP	Advanced calibration fixed license; 1-year update subscription
N1930B-5TP	Advanced calibration transportable license (USB Key); 1-year update subscription
N1930B-6NP	PAM-4 eye diagram networked license; 1-year update subscription
N1930B-6FP	PAM-4 eye fixed license; 1-year update subscription
N1930B-6TP	PAM-4 eye transportable license (USB Key); 1-year update subscription
N1930B-7NP	N-port measurement & analysis networkable license; 1-year update subscription
N1930B-7FP	N-port measurement & analysis fixed license; 1-year update subscription
N1930B-7TP	N-port measurement & analysis transportable license (USB Key); 1-year update subscription

Important notes regarding PLTS software configuration

1. If PLTS Studio is used (PLTS options 1NP, 1FP or 1TP), this will allow data analysis of files up to and including 4 ports (*,s4p Touchstone files). However, if data is to be analyzed from files containing more than 4 ports (for example, 12-port data from a *.s12p Touchstone file), the appropriate PLTS multiport option must be purchased (PLTS options 7NP, 7FP or 7TP).
2. As noted in the sample configurations on pages 16-19 of this technical overview, the VNA firmware options 550 or 551 must be ordered in conjunction with PLTS to work properly as a calibration and measurement system. Option 550 is for applications of 4 ports or less, while option 551 is for applications greater than 4 ports.
3. PLTS option 1xP is required for either 3xP, 5xP, 6xP, or 7xP options.
4. PLTS has an annual update called "SUS" that stands for "Software Update Service". Each new PLTS license comes with 12 months of SUS. After 12 months, a 1 or 2 year SUS must be purchased to receive technical support and new PLTS software updates. If any SUS lapses, then a 2 year SUS must be purchased to re-activate the support and updates.
5. Option 3xP is required for instrument control portions of option 5xP. As noted in 3 above, option 1xP is required for either 3xP, 5xP, 6xP, or 7xP options.
6. Lowest version of firmware that goes through full QA for the PNA is A.09.42.xx. This is the minimum fully supported version as reported in the System Requirement section of the Help file under PLTS Testing.

PLTS SUS (Software Update Service)

If PLTS SUS (Software Update Service) needs to be reordered, it will be necessary to purchase the SUS for each option separately. For example, if the PLTS license has N1930B-1FP (Fixed Analysis), N1930B-3FP (Fixed Measurement) and N1930B-5FP (Fixed Advanced Calibration) options, then the corresponding SUS ordering part numbers will be N1930BU-1FP, N1930BU-3FP and N1930BU-5FP.

Which SUS Extension do I purchase?

PLTS application software uses new licensing capabilities. Besides fixed license and networkable FLEXIm licensing on a shared server, there is also a transportable USB key. The summary of the three licensing options are as follows:

Option xFP Fixed license (default).

Fixed licenses are locked to a single PC through its host ID (e.g., the MAC address) with or without connected system hardware. Fixed licenses do not require any networking or license server processes. A fixed license is also known as a node-locked license.

Option xNP Networkable license.

Networkable licenses allow users to share a single license, or multiple licenses, over a network. The application software may be installed on an unlimited number of PCs with or without connected system hardware. The number of available licenses determines the number of concurrent users. Networkable licenses require a license server and a TCP/IP (or IPX/SPX) connection between clients and server(s). A networkable license is also known as a floating license.

Option xTP Transportable license.

Transportable licenses are locked to a USB key that can be shared among different PCs.

Important licensing notes:

1. File import, file export, calibrations, and measurements greater than 4 ports requires one of the following PLTS options: 7NP, 7FP, or 7TP.

Table 1. Current Software Update Service Part Numbers

Original Product Ordered	SUS Update to Purchase
N1930U (first orders) *If the N1930A was ordered	N1930U-010 (1 year SUS Update) or N1930U-011 (2 year SUS Update)
N1930A-010	N1930U-010 (1 year SUS Update) or N1930U-011 (2 year SUS Update)
N1930A-020	N1930U-020 (1 year SUS Update) or N1930U-021 (2 year SUS Update)
N1930A-LT1	N1930U-LT1 (1 year SUS Update) or N1930U-L12 (2 year SUS Update)
N1930A-LT2	N1930U-LT2 (1 year SUS Update) or N1930U-L22 (2 year SUS Update)
N1930B-xyP x= 1,3,5 or 7 y=F,N, or T	N1930BU-xyP x= 1,3,5 or 7 y=F,N, or T

Note: If SUS is expired, either a 2 year SUS product or quantity 2 of a 1 year SUS product must be ordered to reactivate the expired SUS.

Software License Options

N1930B-1xP – This is the base of all PLTS configurations. This is the UI and analysis functionality for up to 4 port data.

N1930B-3xP – This adds on to a 1xP and allows the software to control the measurement equipment for calibration and measurement for up to 4 port data.

N1930B-5xP – This adds the TRL Cal Kit Wizard, Differential Cross Talk Cal, and Automatic Fixture Removal functionality on to both 1xP and 3xP. If present with 1xP only it allows for post processing, where if present with both (1xP and 3xP) it allows for both the analysis and measurement functionality.

N1930B-6xP – This adds on to any option and allows for PAM-4 eye diagram analysis.

N1930B-7xP – This adds on to both 1xP and 3xP. If present with 1xP it allows for analysis of data files with more than 4 ports, while if present with 3xP it also allows for measurement and calibration control with equipment that has greater than 4 ports. Current limitation is analysis up to 32 ports and measurement to 28 ports.

Possible License Combinations

1xP only – This is an analysis-only license for up to 4 port data.

1xP and 3xP – This is a license combination that allows data analysis, calibration, and measurement of up to 4 ports.

1xP and 5xP – This allows for analysis with the advanced calibration option.

1xP and 7xP – This is a license combination that allows analysis of data files greater than 4 ports (current limit is 32 ports).

1xP, 3xP, and 5xP – This allows for analysis and measurement with the advanced calibration option up to 4 ports.

1xP, 3xP, and 7xP – This is a license combination that allows for analysis, calibration, and measurement for data files and systems greater than 4 port* (current limit is 32 ports).

1xP, 5xP, and 7xP – This allows for analysis of data files greater than 4 ports (current limit is 32 port) with access to the advanced calibration option.

1xP, 3xP, 5xP and 7xP – This is a license combination that allows for analysis, calibration, and measurement for data files and systems greater than 4 port* (current limit is 32 ports) with the advanced calibration option.

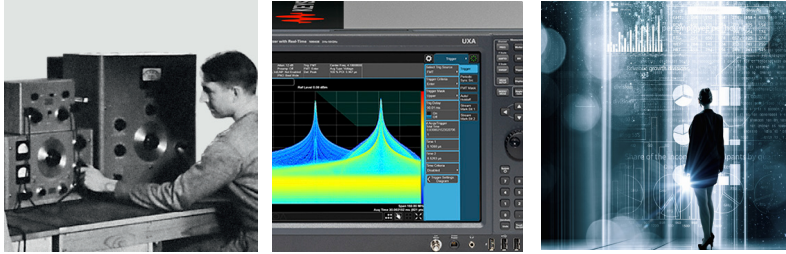
Note: N1930B-6xP can be added to any option above.

* For a PNA-based system to perform measurements and calibrations greater than 4 ports, Option 551 is required on the PNA.

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